ZETTA SD NAND Product Datasheet

4Gb/8Gb/16Gb/32Gb/64Gb
pSLC/MLC

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1. Product Description

ZETTA SD NAND is an embedded storage based on pSLC/MLC NAND Flash and SD controller. This product has many advantages comparing to raw NAND, it has embedded bad block management, and stronger embedded ECC.

SD NAND consists of NAND flash and a high-performance controller. 3.3V supply voltage is required for the NAND area (VCC). According to SD protocol, SD NAND below 16Gb uses the SD2.0 protocol, so 4Gb/8Gb/16Gb SD NAND is fully compliant with SD2.0 interface, 32Gb/64Gb SD NAND is fully compliant with SD3.0 interface, which is utilized by most of general CPU. The advantages of the SD NAND include high quality, low power consumption and cost performance.

2. Product Listm

Capacity	Part number	Package	Size	Temp. Range
4Gb -pSLC	ZDSD04GLQEAG	LGA8x2 (Land Grid Array)	9x10mm	-25°C to +85°C
8Gb -pSLC	ZDSD08GLQEAG	LGA8x2 (Land Grid Array)	9x10mm	-25°C to +85°C
16Gb -pSLC	ZDSD16GLQEAG	LGA8x2 (Land Grid Array)	9x10mm	-25°C to +85°C
32Gb -pSLC	ZDSD32GLQEAG	LGA8x2 (Land Grid Array)	9x10mm	-25°C to +85°C
64Gb -MLC	ZDSD64GLQEAG	LGA8x2 (Land Grid Array)	9x10mm	-25°C to +85°C

3. Features

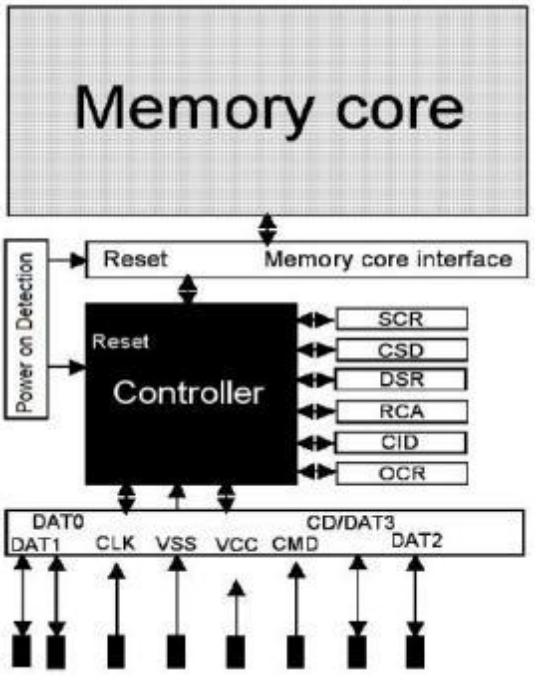
SD3.0 interface:

- √ Support up to 200Mhz clock frequency
- √ Support 1/4 bit mode
- √ Built-in HW ECC Engine and highly reliable NAND management mechanism
- √ High Speed model, Speed class 4/class 6/class 8/class10 supported.
- √ Smaller package LGA8 (Land Grid Array)
- √ Operation Conditions Temperature Range: Extended Ta = -25°C to +85°C
- √ Storage Conditions Temperature Range: Tstg = -55°C to +105°C

SD2.0 interface:

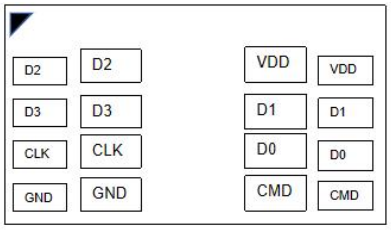
- √ Support up to 50Mhz clock frequency
- √ Support 1/4 bit mode
- √ Built-in HW ECC Engine and highly reliable NAND management mechanism
- √ High Speed model supported.
- √ Smaller package LGA8 (Land Grid Array)
- √ Operation Conditions Temperature Range: Extended Ta = -40°C to +85°C
- √ Storage Conditions Temperature Range: Tstg = -55°C to +150°C

4. Block Diagram

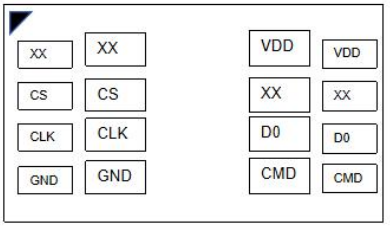


5. Pin Assignments(SD Mode& SPI Mode)

Top view through package



SD Mode



SPI Mode

SD 4-bit mode		SD 1-bit mode		SPI mode	
CD/DAT[3]	Data line 3	N/C	Not Used	CS	Card Select
CMD	Command line	CMD	Command line	DI	Data input
GND	Ground	GND	Ground	GND	Ground
VDD	Supply voltage	VDD	Supply voltage	VDD	Supply voltage
CLK	Clock	CLK	Clock	SCLK	Clock
DAT[0]	Data line 0	DATA	Data line	DO	Data output
DAT[1]	Data line 1	N/C	Not Used	NC	Not Used
DAT[2]	Data line 2	N/C	Not Used	NC	Not Used

6. Bus Protocol

6.1 SD Bus Mode protocol

The SD bus allows the dynamic configuration of the number of data line from 1 to 4 Bi-directional data signal. After power up by default, the SD card will use only DAT0. After initialization, host can change the bus width.

Multiplied SD cards connections are available to the host. Common VDD, VSS and CLK signal connections are available in the multiple connections. However, Command, Respond and Data lined (DAT0-DAT3) shall be divided for each device from host.

This feature allows easy trade off between hardware cost and system performance. Communication over the SD bus is based on command and data bit stream initiated by a start bit and terminated by stop bit.

Command: a command is a token that starts an operation. A command is sent from the host either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line.

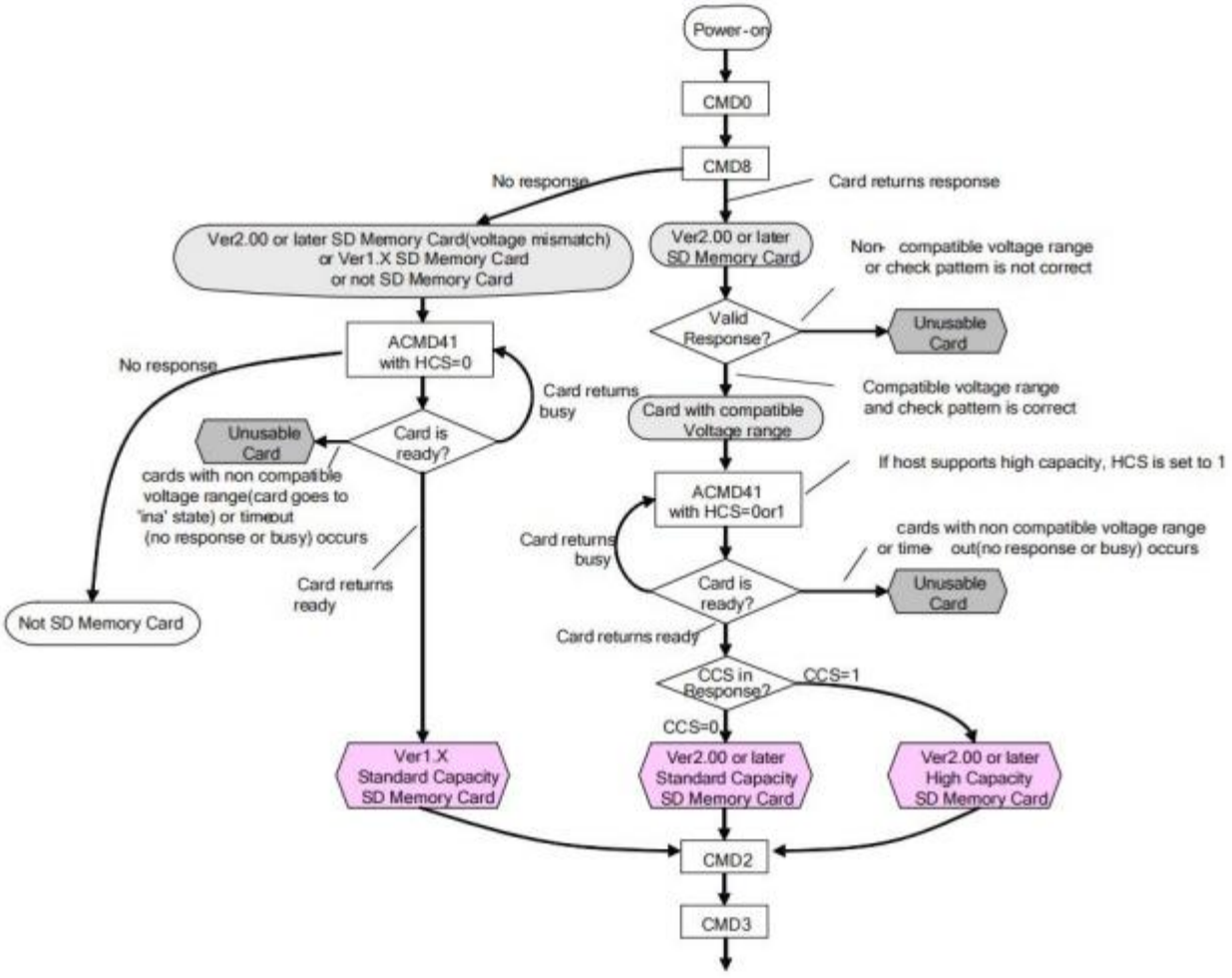
Response: a response is a token that is sent from an addressed card, or (synchronously) from all connected cards, to the host as an answer to a previously received command. A response is transferred serially on the CMD line.

Data: data can be transferred from the card to the host or vice versa. Data is transferred via the data lines.

6.2 Card Initialization and Identification Process

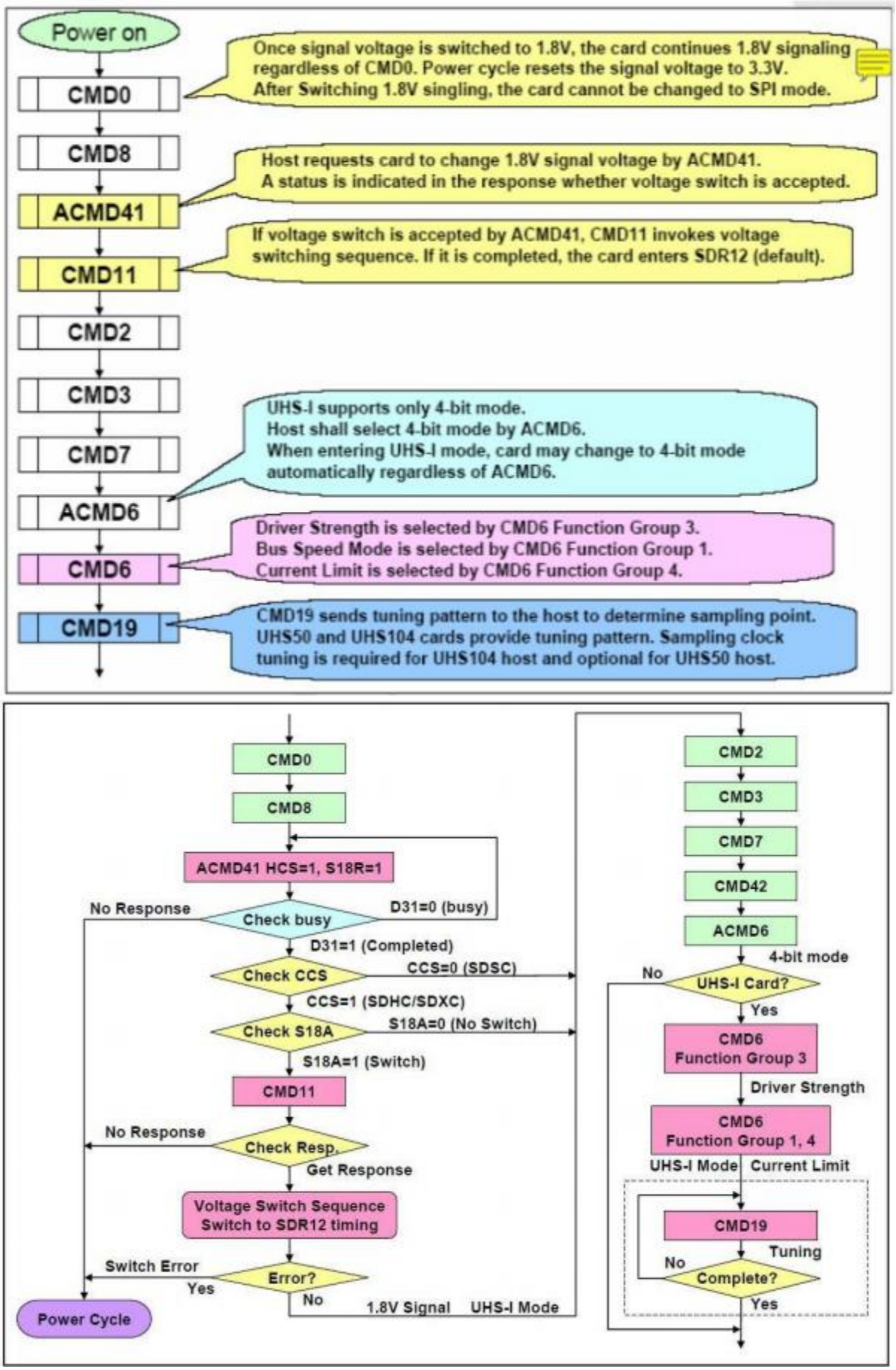
6.2.1 SD MODE:

After the bus is activated the host starts card initialization and identification process. The initialization process starts with SD_SEND_OP_COND (ACMD41) by setting its operational conditions and the HCS bit in the OCR. The HCS (Host Capacity Support) bit set to 1 indicates that the host supports High Capacity SD Memory card. The HCS (Host Capacity Support) bit set to 0 indicates that the host does not support High Capacity SD Memory card.



Card Initialization and Identification Flow (SD2.0 mode)

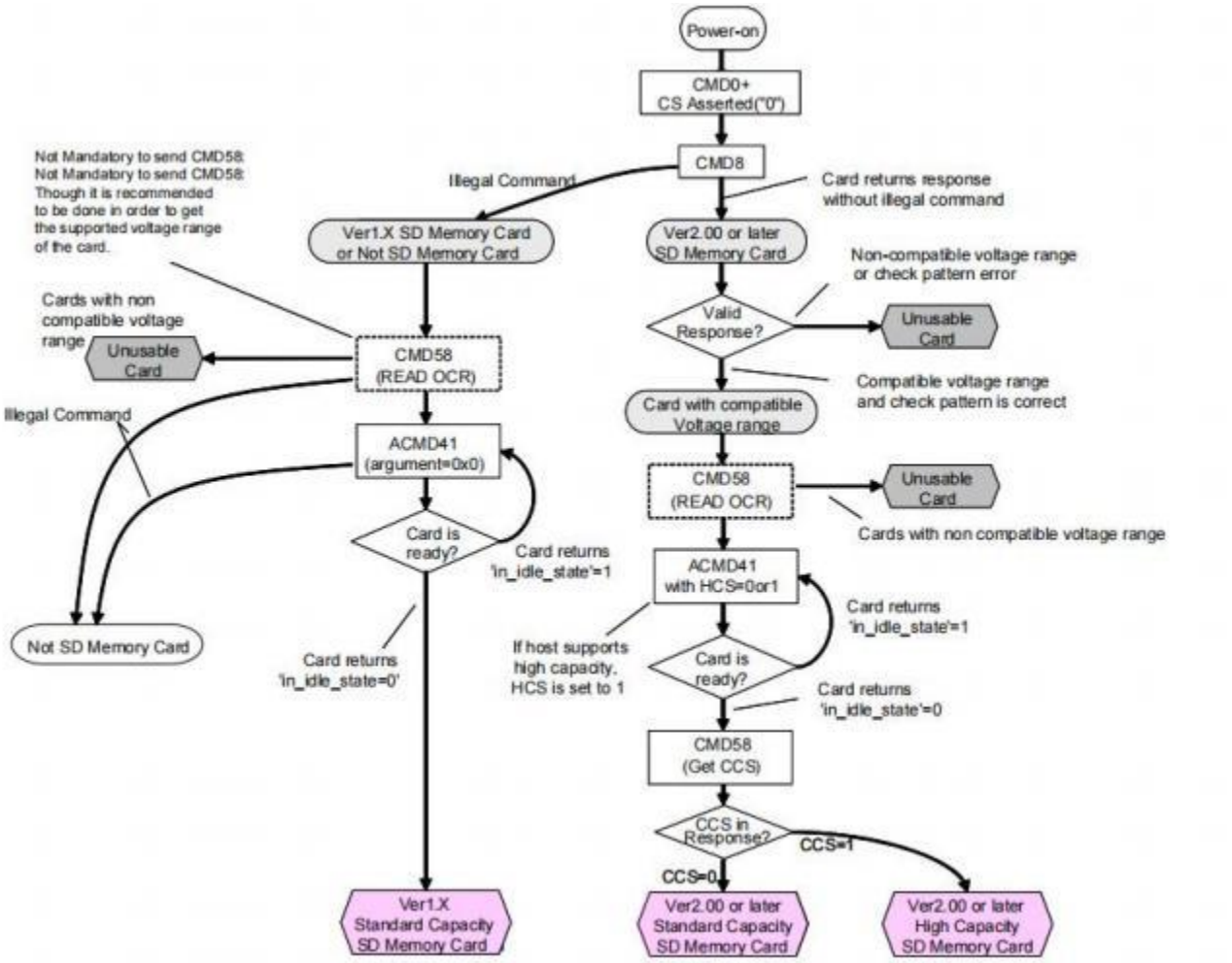
SD3.0 initial flow for UHS-I(IO 1.8v) switch



Card Initialization and Identification Flow (SD3.0 mode)

6.2.2 SPI MODE:

The SD Card will enter SPI mode if the CS signal is asserted (negative) during the reception of the reset command (CMD0). If the card recognizes that the SD mode is required it will not respond to the command and remain in the SD mode. If SPI mode is required, the card will switch to SPI and respond with the SPI mode R1 response. The only way to return to the SD mode is by entering the power cycle. In SPI mode, the SD Card protocol state machine in SD mode is not observed. All the SD Card commands supported in SPI mode are always available.



SPI Mode Initialization Flow

6.3 Wide Bus Selection/Deselection

Wide Bus (4 bit bus width) operation mode may be selected/deselected using ACMD6. The default bus width after power up or GO_IDLE (CMD0) is 1 bit bus width.

In order to change the bus width two conditions shall be met:

a) The card is in ‘tran state‘ (no data is transferred).

b) The card is not locked

A locked card will responds to ACMD6 as illegal command.

6.4 DC Characteristics

DC Characteristics

Item		Symbol	MIN.	TYP	MAX.	Unit	Note
Supply Voltage		VDD	2.7		3.6	V	
Input Voltage	High Level	VIH	VDD×0.625		VDD+0.3	V	
	Low Level	VIL	VSS-0.3		VDD×0.25	V	
Output Voltage	High Level	VOH	VDD×0.75		–	V	IOH=-2mA , VDD=VDD min
	Low Level	VOL	–		VDD×0.125	V	IOL=2mA , VDD=VDD min
Standby Current		ICC1	–	0.17	0.2	mA	VDD = 3.3V, Clock STOP, Ta= 2 5 ℃
Operation Current (*)	Write	ICC2	–	TBD	–	mA	3.3V/ 50MHz
	Read		–	TBD	–		
Input Voltage Setup Time		Vrs	–		250	ms	From 0V to VDD min

Peak Voltage and Leak Current

Item	Symbol	Min.	Max.	Unit	Note
Peak voltage on all lines		-0.3	VDD+0.3	V	
Input Leakage Current for all pins		-10	10	uA	
Output Leakage Current for all outputs		-10	10	uA	

Signal Capacitance

Item	Symbol	Min.	Max.	Unit	Note
Pull up Resistance	RCMD RDAT	10	100	kΩ	
Total bus capacitance for each signal line	CL	—	40	pF	1 card CHOST+CBUS≤30pF
Card capacitance for signal pin	CCARD	—	10	pF	
Pull up Resistance inside card (pin1)	RDAT3	10	90	kΩ	
Capacity Conneted to Power line	CC	—	5	uF	

7 Internal Information

7.1 Registers

The SD NAND has six registers and SD Status information: OCR, CID, CSD, RCA,DSR, SCR and SD Status.
DSR IS NOT SUPPORTED in this card.

SD card Registers

Resister Name	Bit Width	Description
OCR	32	Operation Conditions (VDU Voltage Profile and Busy Status
CID	128	Card Identification information
CSD	128	Card specific information
RCA	16	Relative CardAddress
DSR	16	Not Implemented (Programmable Card Driver): Driver Stage Register
SCR	64	SDMemoryCards special features
SD Status	512	Status bits and Card features

7.1.1 OCR Register

This 32-bit register describes operating voltage range and status bit in the power supply.

OCR register definition

OCR bit	VDD voltage window	Initial
31	Card power up status bit(busy)	"0" = busy "1" =
30	Card Capacity Status	"0"= SD Memory Card
29-25	reserved	All 0
24	Switching to 1.8V Accepted(S18A)	0/1
23	3.6 - 3.5	1
22	3.5 - 3.4	1
21	3.4 - 3.3	1
20	3.3 - 3.2	1
19	3.2 - 3.1	1
18	3.1 - 3.0	1
17	3.0 - 2.9	1
16	2.9 - 2.8	1
15	2.8 - 2.7	1
14	Reserved	0
13	Reserved	0
12	Reserved	0
11	Reserved	0
10	Reserved	0
9	Reserved	0
8	Reserved	0
7	Reserved for Low Voltage Range	0
6	Reserved	0
5	Reserved	0
4	Reserved	0
3-0	reserved	All 0

1) This bit is valid only when the card power up status bit is set.
2) This bit is set to LOW if the card has not finished the power up routine.

7.1.2 CID Register

The Card IDentification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual Read/Write (RW) card shall have a unique identification number. The structure of the CID register is defined in the following paragraphs:

Name	Field	Width	CID-slice
Manufacturer ID	MID	8	[127:120]
OEM/Application ID	OID	16	[119:104]
Product name	PNM	40	[103:64]
Product revision	PRV	8	[63:56]
Product serial number	PSN	32	[55:24]
Reserved	-	4	[23:20]
Manufacturing date	MDT	12	[19:8]
CRC7 checksum	CRC	7	[7:1]
Not used, always 1	-	1	[0:0]

7.1.3 CSD Register

CSD is Card-Specific Data register provides information on 128bit width. Some field of this register can writable by PROGRAM_CSD (CMD27).

Field	Width	Cell Type	CSD Slice	Initial Value
CSD_STRUCTURE	2	R	[127:126]	01b or 00b
reserved	6	R	[125:120]	000000b
TAAC	8	R	[119:112]	00001110b
NSAC	8	R	[111:104]	00000000b
TRAN_SPEED	8	R	[103:96]	xxxb
CCC	12	R	[95:84]	010110110101b
READ_BL_LEN	4	R	[83:80]	1001b
READ_BL_PARTIAL	1	R	[79:79]	0b
WRITE_BLK_MISALIG	1	R	[78:78]	0b
READ_BLK_MISALIGN	1	R	[77:77]	0b
DSR_IMP	1	R	[76:76]	0b
reserved	6	R	[75:70]	000000b
C_SIZE	22	R	[69:48]	xxxb
reserved	1	R	[47:47]	0b
ERASE_BLK_EN	1	R	[46:46]	1b
SECTOR_SIZE	7	R	[45:39]	1111111b
WP_GRP_SIZE	7	R	[38:32]	0000000b
WP_GRP_ENABLE	1	R	[31:31]	0b
reserved	2	R	[30:29]	00b
R2W_FACTOR	3	R	[28:26]	010b
WRITE_BL_LEN	4	R	[25:22]	1001b
WRITE_BL_PARTIAL	1	R	[21:21]	0b
reserved	5	R	[20:16]	00000b
FILE_FORMAT_GRP	1	R/W(1(1)	[15:15]	0b
COPY	1	R/W(1)	[14:14]	0b
PERM_WRITE_PROTE	1	R/W(1)	[13:13]	0b
TMP_WRITE_PROTEC	1	R/W	[12:12]	0b
FILE_FORMAT	2	R	[11:10]	00b
reserved	2	R	[9:8]	00b
CRC	7	R/W	[7:1]	1101011b
not used, always'1'	1	-	[0:0]	1b

Cell Type:R: Read Only, R/W: Writable and Readable, R/W(1): One-time Writable / Readable

Note: Erase of one data block is not allowed in this card. This information is indicated by "ERASE_BLK_EN" .

Host System should refer this value before one data block size erase.

7.1.4 RCA Register

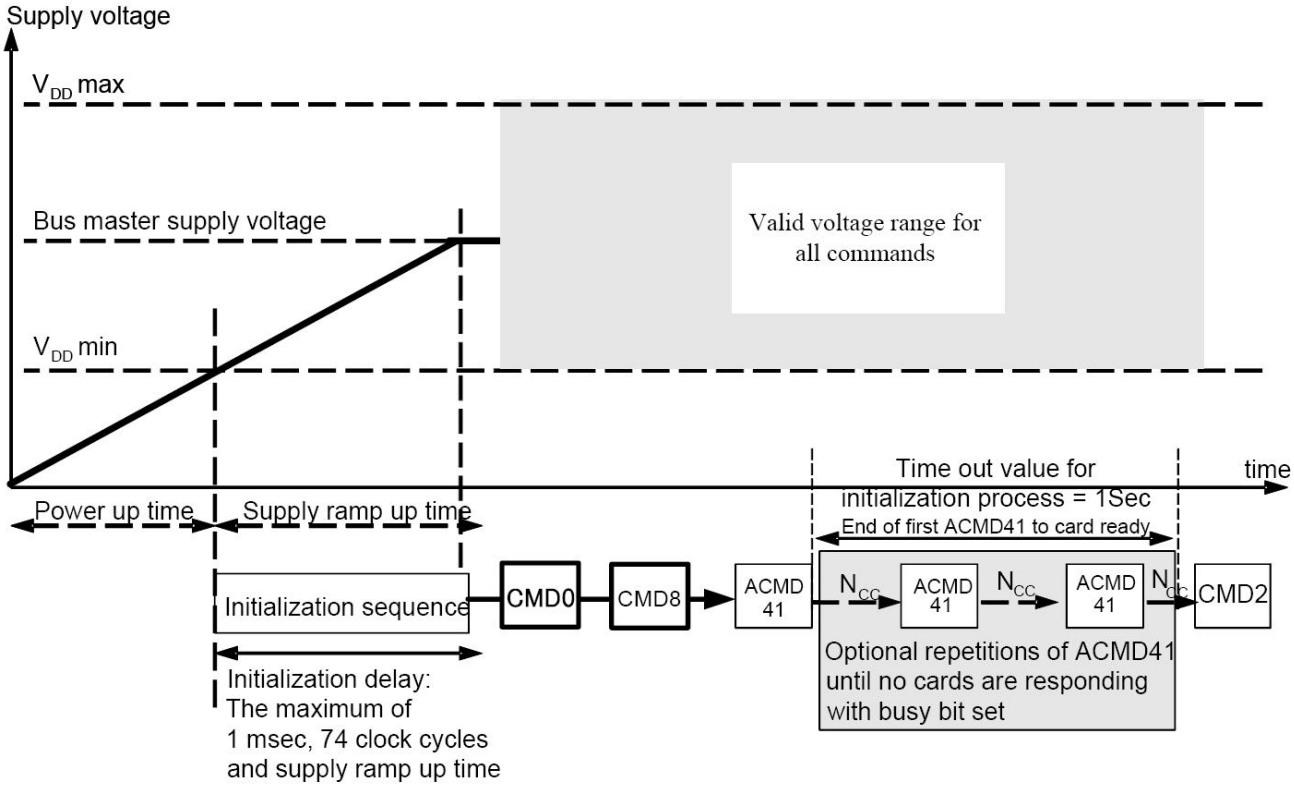
The writable 16-bit relative card address register carries the card address that is published by the card during the card identification. This address is used for the addressed host-card communication after the
card identification procedure. The default value of the RCA register is 0x0000. The value 0x0000 is reserved to set all cards into the Stand-by State with CMD7.

8 Power Scheme

8.1 Power Up

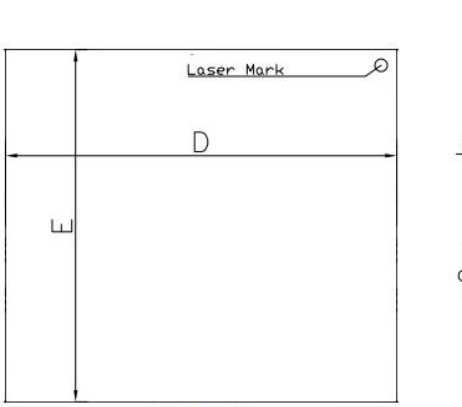
Power up time is defined as voltage rising time from 0 volt to VDD min and depends on application parameters such as the maximum number of SD Cards, the bus length and the characteristic of the power supply unit.

Supply ramp up time provides the time that the power is built up to the operating level (the bus master supply voltage) and the time to wait until the SD card can accept the first command,The host shall supply power to the card so that the voltage is reached to Vdd_min within 250ms and start to supply at least 74 SD clocks to the SD card with keeping CMD line to high. In case of SPI mode, CS shall be held to high during 74 clock cycles.

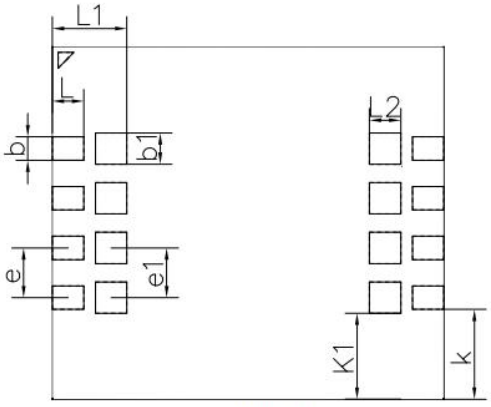


9. Package Dimensions

LGA16 9x10mm (Land Grid Array)



TOP VIEW



BOTTOM VIEW

COMMON DIMENSIONS (UNITS OF MEASURE=MILLIMETER)			
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
K1	2.14	2.19	2.24
K	2.25	2.30	2.35
b1	0.75	0.80	0.85
b	0.55	0.60	0.65
L2	0.75	0.80	0.85
L1	1.85	1.90	1.95
L	0.75	0.80	0.85
E	8.95	9.00	9.05
D	9.95	10.00	10.05
A	8.95	0.90	0.95
e	1.27BSC		
e1	1.27BSC		



10. Ordering Information

The ordering part number is formed by a valid combination of the following

