MLC e·MMC™ and Mobile LPDDR3 221-Ball MCP

Features

- MLC NAND Flash in *e*·MMC
- RoHS-compliant, "green" package
- Separate *e*·MMC and LPDDR3 interfaces
- Space-saving multichip package
- Low-voltage operation VDD (1.70–1.95V)
- Dual voltage VCCQM (1.70–1.95V, 2.7–3.6V)
- Wireless temperature range: –30°C to +85°C

e-MMC-Specific Features

- JEDEC/MMC standard version 4.51-compliant SPI mode not supported[1]
  - Advanced 11-signal interface
  - x1, x4, and x8 I/Os, selectable by host
  - SDR/DDR modes up to 52 MHz clock speed
  - Real-time clock and high-speed HS200 mode
  - Command classes: class 0 (basic); class 2 (block read); class 4 (block write); class 5 (erase); class 6 (write protection); class 7 (lock card)
  - Temporary, permanent, and power-on write protection
  - Boot operation (high-speed boot)
  - Sleep mode
  - Hardware reset signal
  - Replay-protected memory block (RPMB)
  - Secure erase and secure trim
  - Multiple partitions with enhanced attribute
  - High-priority interrupts (HPI)
  - Background operations
  - Reliable write
  - Discard and sanitize

  Extended partitioning
  - Context ID and data TAG
  - Packed commands
  - Thermal specification
  - Cache
  - Backward compatible with previous MMC
- ECC and block management implemented

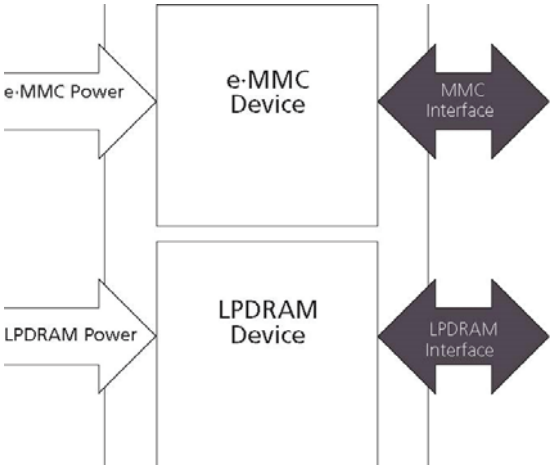


Figure 1: MCP Block Diagram

Mobile-LPDDR3-Specific Features

- Ultra-low-voltage 1.2V core power supply
- 1.2V HSUL-compatible inputs
- Frequency range
  – 800–10 MHz (data rate range: 1600–20 Mb/s/pin)
- Programmable read and write latencies
- Programmable burst lengths: 8
- Partial-array self refresh (PASR)

- Deep power-down (DPD) mode
- Selectable output drive strength
- Adjustable clock frequency and clock stop capabilities
- On-die termination (ODT)

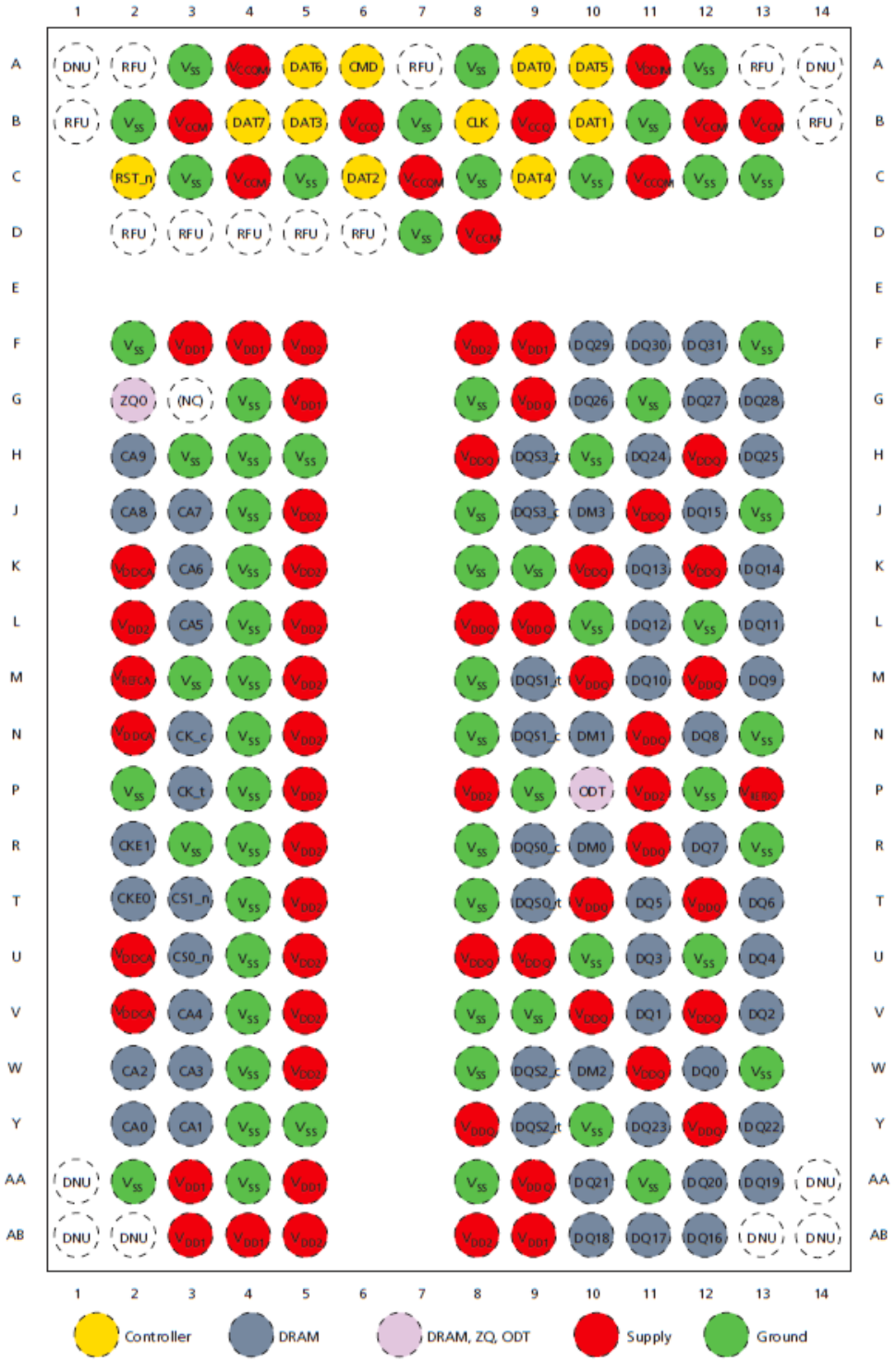
Notes: 1. See unsupported JEDEC features in Product Revision. JEDEC Standard No. 84-B451 specification is at www.jedec.org/sites/default/ files/docs/JESD84-B451.pdf.

1. MCP General Description

Zetta MCP products combine *e*·MMC and Mobile LPDRAM devices in a single MCP. These products target mobile applications with low-power, high-performance, and minimal package-footprint design requirements.
The *e*·MMC and Mobile LPDRAM devices are packaged with separate interfaces (no shared address, control, data, or power balls). This bus architecture supports an optimized interface to processors with separate *e*·MMC and Mobile LPDRAM buses.
The *e*·MMC and Mobile LPDRAM devices have separate core power connections and share a common ground (that is, VSS is tied together on the two devices).
The bus architecture of this device also supports separate *e*·MMC and Mobile LPDRAM functionality without concern for device interaction.

2. Ball Assignments

Figure 2: 221-Ball VFBGA (e • MMC; x32 LPDDR3) Ball Assignments



3. Ball Descriptions

Table 1: e • MMC Ball Descriptions

Symbol	Type	Description
CLK	Input	**Clock:** Each cycle directs a 1-bit transfer on the command and DAT lines.
CMD	I/O	**Command:** A bidirectional channel used for device initialization and command transfers. Command has two operating modes: 1) Open drain for initialization. 2) Push-pull for fast command transfer.
DAT[7:0]	I/O	**Data bus:** Bidirectional channel used for data transfer.
RST_n	Input	Reset
V_{CCM}	Supply	**V_{CCM}:** NAND I/F I/O and NAND power supply (2.70–3.6V).
V_{CCQM}	Supply	**V_{CCQM}:** e·MMC controller core and e·MMC I/F I/O power supply (1.70–1.95V).
V_{DDIM}	–	**V_{DDIM}:** The internal regulator connection to an external decoupling capacitor (see the Capacitor and Resistance Specifications table).

Table 2: x32 LPDDR3 Ball Descriptions

Symbol	Type	Description
CA[9:0]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
CK_t, CK_c	Input	**Clock:** Differential clock inputs. All CA inputs are sampled on both rising and falling edges of CK. CS and CKE inputs are sampled at the rising edge of CK. AC timings are referenced to clock.
CKE[1:0]	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is considered part of the command code. CKE is sampled at the rising edge of CK. For a single-die LPDDR3 MCP, only CKE0 is used. CKE1 is used in case of dual-die LPDDR3 MCP.
CS[1:0]_n	Input	**Chip select:** Considered part of the command code and is sampled at the rising edge of CK. For a single-die LPDDR3 MCP, only CS0_n is used. CS1_n is used in case of dual-die LPDDR3 MCP.
DM[3:0]	Input	**Input data mask:** DM is an input mask signal for write data. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. DM[3:0] is DM for each of the four data bytes, respectively.
ODT	Input	**On-Die Termination:** This signal enables and disables termination on the DRAM DQ bus according to the specified mode register settings.

Table 2: x32 LPDDR3 Ball Descriptions (Continued)

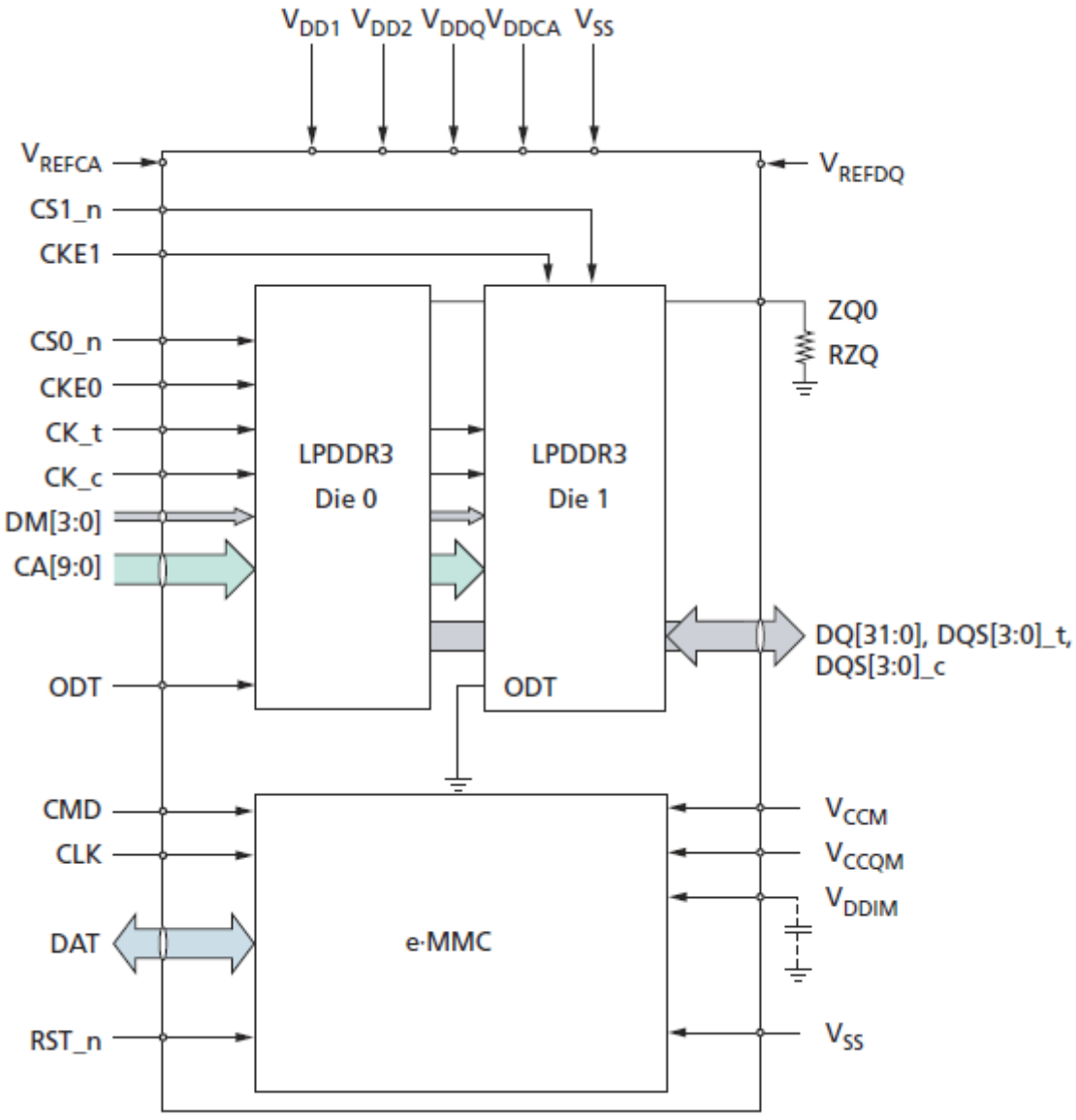
Symbol	Type	Description
DQ[31:0]	I/O	**Data input/output:** Bidirectional data bus.
DQS[3:0]_t, DQS[3:0]_c	I/O	**Data strobe:** The data strobe is bidirectional (used for read and write data) and complementary (DQS_t and DQS_c). It is edge-aligned output with read data and centered input with write data. DQS[3:0]_t/DQS[3:0]_c is DQS for each of the four data bytes, respectively.
V_{DDQ}	Supply	**DQ power supply:** Isolated on the die for improved noise immunity.
V_{DDCA}	Supply	**Command/address power supply:** Command/address power supply.
V_{DD1}	Supply	**Core power:** Supply 1.
V_{DD2}	Supply	**Core power:** Supply 2.
V_{REFCA}, V_{REFDQ}	Supply	**Reference voltage:** V_{REFCA} is reference for command/address input buffers, V_{REFDQ} is reference for DQ input buffers.
ZQ0	Reference	**External impedance (240 ohm):** This signal is used to calibrate the device output impedance.

Table 3: Non-Device-Specific Descriptions

Symbol	Type	Description
VSS	Supply	**VSS:** Shared ground.
DNU	–	**Do not use:** Must be grounded or left floating.
NC	–	**No connect:** Not internally connected.
(NC)	–	**No connect:** Balls indicated as (NC) are no connects; however, they could be connected together internally.

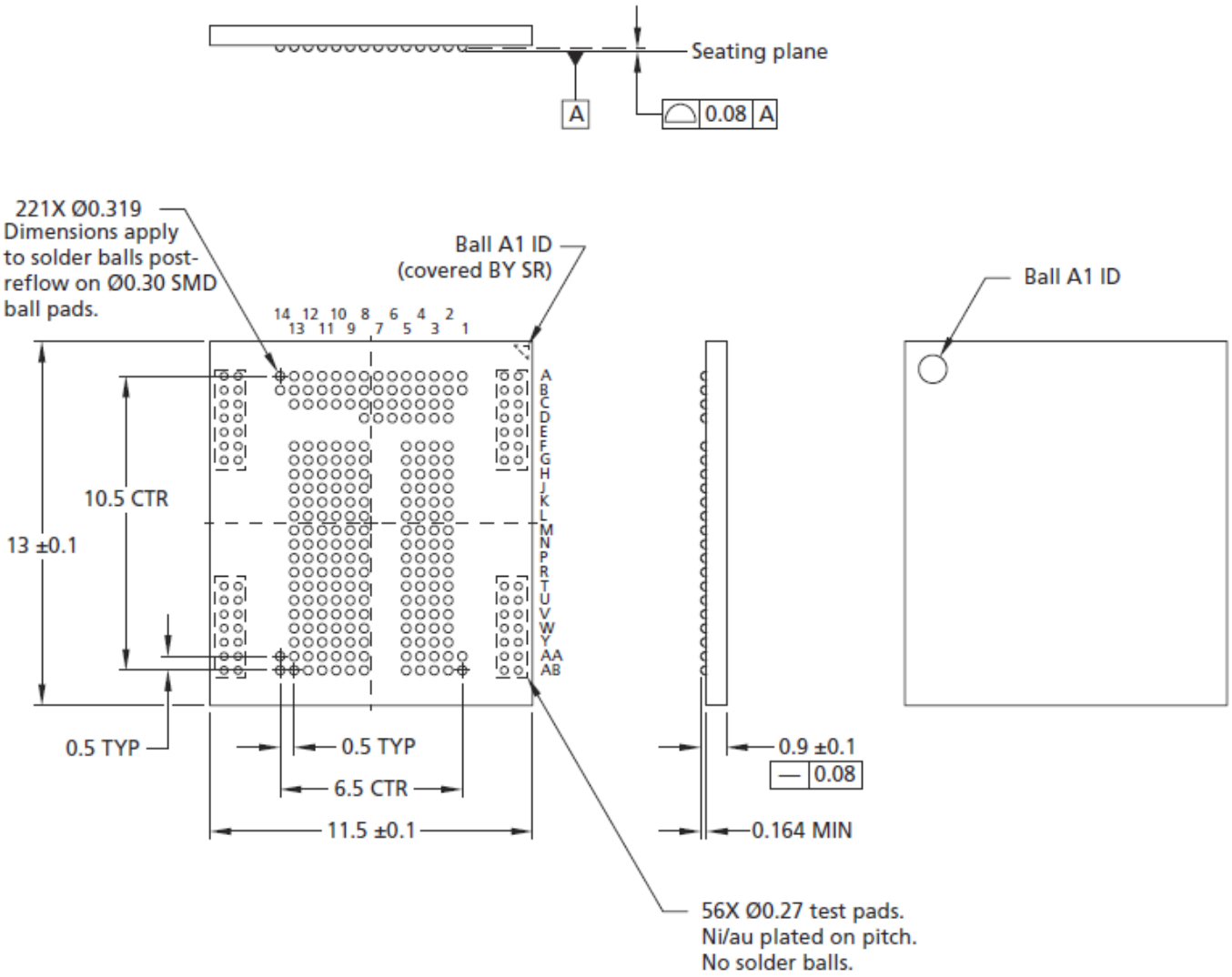
4. Device Diagrams

Figure 4: Functional Block Diagram – e • MMC and Dual-Die x32 LPDDR3



5. Package Dimensions

Figure 5: 221-Ball VFBGA



Notes: 1. Solder ball material: LF35 with Cu OSP ball pads (98.25% Sn, 1.2% Ag, 0.5% Cu, 0.05% Ni).
2. All dimensions are in millimeters.

6. Revision History

Doc. No.	Date	Comments
	12/2015	Initial document release.