Zetta 4Gbit DDR3L SDRAM

Datasheet

Features

• VDD=VDDQ=1.35V + 0.100 / - 0.067V

• Fully differential clock inputs (CK, $\overline{CK}$) operation

• Differential Data Strobe (DQS, $\overline{DQS}$)

• On chip DLL align DQ, DQS and $\overline{DQS}$ transition with CK transition

• DM masks write data-in at the both rising and falling edges of the data strobe

• All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock

• Programmable CAS latency 5, 6, 7, 8, 9, 10, 11, 13 supported

• Programmable additive latency 0, CL-1, and CL-2 supported

• Programmable CAS Write latency (CWL) = 5, 6, 7, 8, 9

• Programmable burst length 4/8 with both nibble sequential and interleave mode

• BL switch on the fly

• 8banks

• Average Refresh Cycle (Tcase of 0 ℃ ~ 95 ℃) - 7.8 μs at 0℃ ~ 85 ℃ - 3.9 μs at 85℃ ~ 95 ℃

• JEDEC standard 96ball FBGA

• Driver strength selected by EMRS

• Dynamic On Die Termination supported

• Asynchronous RESET pin supported

• ZQ calibration supported

• Write Levelization supported

• 8 bit pre-fetch

• This product in compliance with the RoHS directive.

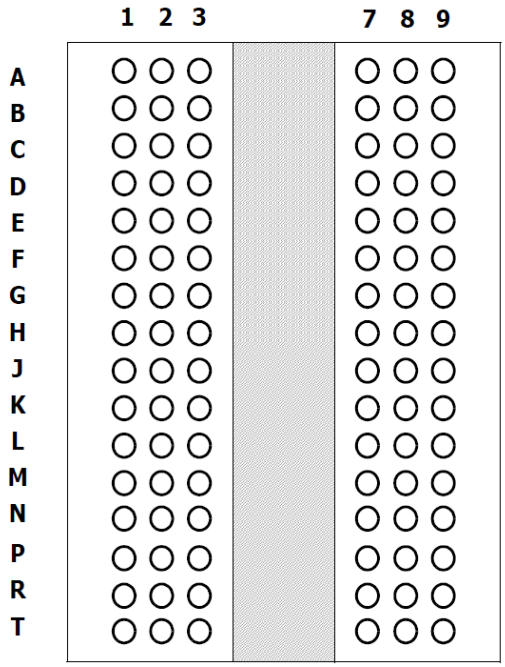
1. Description

Zetta DDR3L SDRAM is a 4Gbit low power Double Data Rate III (DDR3L) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density, high bandwidth and low power operation at 1.35V. DDR3L SDRAM provides backward compatibility with the 1.5V DDR3 based environment without any changes. Zetta 4Gb DDR3L SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 8-bit prefetched to achieve very high bandwidth.

2. Package Ballout/Mechanical Dimension

x16 Package Ball out (Top view): 96ball FBGA Package

	1	2	3	4	5	6	7	8	9	
A	VDDQ	DQU5	DQU7				DQU4	VDDQ	VSS	A
B	VSSQ	VDD	VSS				$\overline{\text{DQSU}}$	DQU6	VSSQ	B
C	VDDQ	DQU3	DQU1				DQSU	DQU2	VDDQ	C
D	VSSQ	VDDQ	DMU				DQU0	VSSQ	VDD	D
E	VSS	VSSQ	DQL0				DML	VSSQ	VDDQ	E
F	VDDQ	DQL2	DQSL				DQL1	DQL3	VSSQ	F
G	VSSQ	DQL6	$\overline{\text{DQSL}}$				VDD	VSS	VSSQ	G
H	VREFDQ	VDDQ	DQL4				DQL7	DQL5	VDDQ	H
J	NC	VSS	$\overline{\text{RAS}}$				CK	VSS	NC	J
K	ODT	VDD	$\overline{\text{CAS}}$				$\overline{\text{CK}}$	VDD	CKE	K
L	NC	$\overline{\text{CS}}$	$\overline{\text{WE}}$				A10/AP	ZQ	NC	L
M	VSS	BA0	BA2				NC	VREFCA	VSS	M
N	VDD	A3	A0				A12/$\overline{\text{BC}}$	BA1	VDD	N
P	VSS	A5	A2				A1	A4	VSS	P
R	VDD	A7	A9				A11	A6	VDD	R
T	VSS	$\overline{\text{RESET}}$	A13				A14	A8	VSS	T
	1	2	3	4	5	6	7	8	9	



(Top View: See the balls through the Package)

○ Populated ball
+ Ball not populated

3. Pin Functional Descriptions

Symbol	Type	Function
CK	Input	Clock: All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK.
CKE, (CKE0), (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank).CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK,ODT and CKE, are disabled during powerdown. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS, (CS0), (CS1), (CS2), (CS3)	Input	Chip Select: All commands are masked when CS is registered HIGH. CS provides for external Rank selection on systems with multiple Ranks. CS is considered part of the command code.
ODT, (ODT0), (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, DQS and DM/TDQS, NU/TDQS (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x4/x8 configurations. For x16 configuration, ODT is applied to each DQ, DQSU, DQSU, DQSL, DQSL, DMU, and DML signal. The ODT pin will be ignored if MR1 is programmed to disable ODT.
RAS. CAS. WE	Input	Command Inputs: RAS, CAS and WE (along with CS) define the command being entered.
DM, (DMU), (DML)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS/TDQS is enabled by Mode Register A11 setting in MR1.
BA0 - BA2	Input	Bank Address Inputs: BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS cycle.
A0 - A15	Input	Address Inputs: Provide the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/BC have additional functions, see below).The address inputs also provide the op-code during Mode Register Set commands.

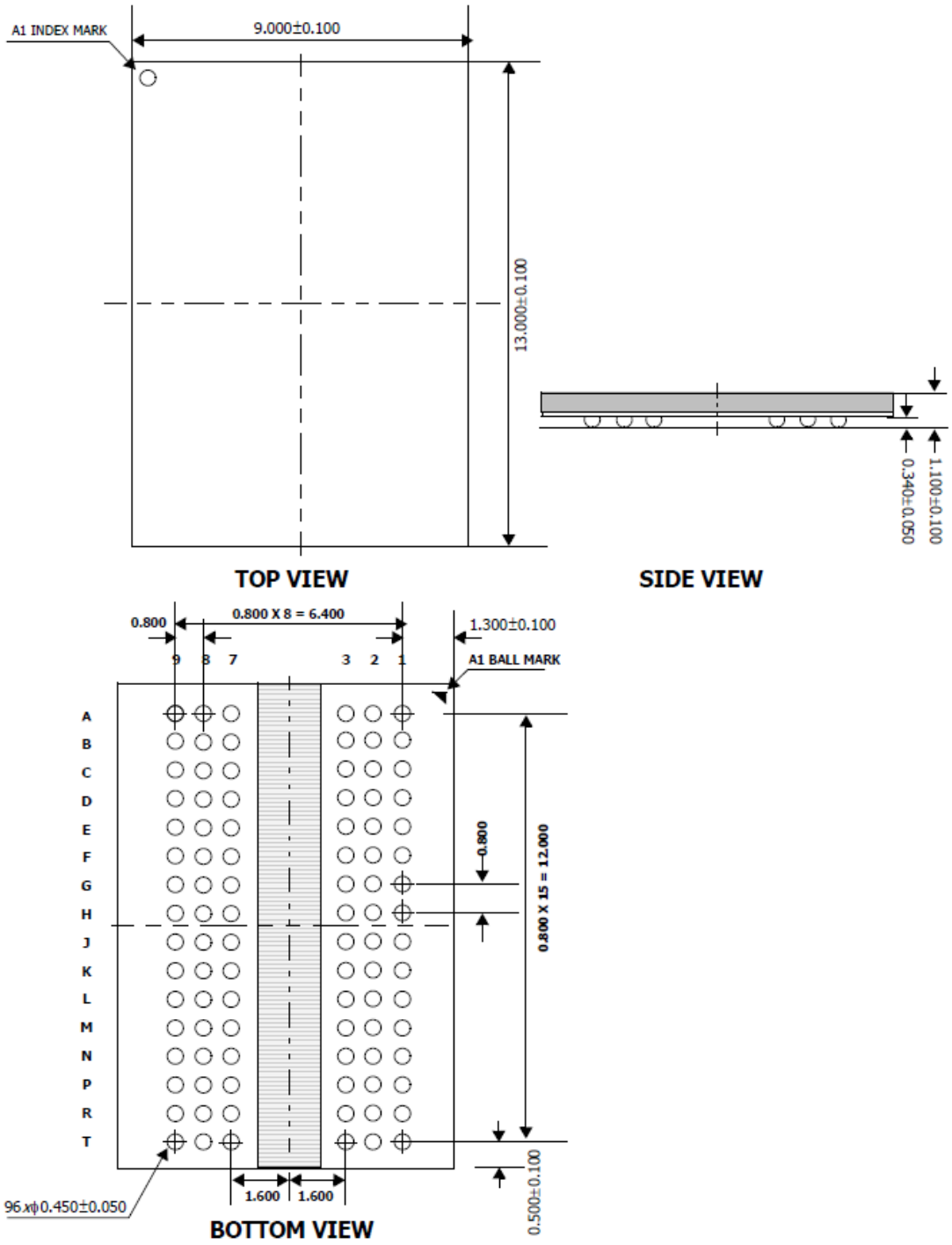
Symbol	Type	Function
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge).A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC	Input	Burst Chop: A12 / BC is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET	Input	Active Low Asynchronous Reset: Reset is active when RESET is LOW, and inactive when RESET is HIGH. RESET must be HIGH during normal operation. RESET is a CMOS rail-to-rail signal with DC high and low at 80% and 20% of VDD, i.e. 1.20V for DC high and 0.30V for DC low.
DQ	Input / Output	Data Input/ Output: Bi-directional data bus.
DQU, DQL, DQS, DQSU, DQSL	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS, DQSL, and DQSU are paired with differential signals DQS, DQSL, and DQSU, respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
TDQS	Output	Termination Data Strobe: TDQS/TDQS is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS/TDQS that is applied to DQS/DQS. When disabled via mode register A11 = 0 in MR1, DM/TDQS will provide the data mask function and TDQS is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
NC		No Connect: No internal electrical connection is present.
NF		No Function
V_{DDQ}	Supply	DQ Power Supply: 1.35 V +0.100/- 0.067 V
V_{SSQ}	Supply	DQ Ground
V_{DD}	Supply	Power Supply: 1.35 V +0.100/- 0.067 V
V_{SS}	Supply	Ground
V_{REFDQ}	Supply	Reference voltage for DQ
V_{REFCA}	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration

4. ROW AND COLUMN ADDRESS TABLE

Configuration	256Mb x 16
# of Banks	8
Bank Address	BA0 - BA2
Auto precharge	A10/AP
BL switch on the fly	A12/BC
Row Address	A0 - A14
Column Address	A0 - A9
Page size	2 KB

5. Package Dimensions

Package Dimension(x16): 96Ball Fine Pitch Ball Grid Array Outline



6. Revision History

Doc. No.	Date	Comments
	01/2016	Initial document release.