64 Megabit Serial Flash Memory with 4Kbytes Uniform Sector

ZD25Q64

FEATURES

Family of SPI Flash Memories

- ZD25Q: 64M-bit / 8M-byte
- Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
- Dual SPI: CLK, /CS, IO_0, IO_1, /WP, /Hold
- Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3

Flexible Architecture with 4KB sectors

- Uniform Sector Erase (4K-bytes)
- Uniform Block Erase (64K-bytes)
- Program 1 to 256 byte per programmable page

Highest Performance Serial Flash

- 108MHz Standard/Dual/Quad SPI clocks
- More than 100,000 erase/program cycles
- More than 20-year data retention

Advanced Security Features

- Write protect all/portion of memory via software
- Enable/Disable protection with WP# Pin
- 64-Byte Security Registers With OTP Locks(1)
- Discoverable parameters(SFDP) register(1)

Low Power consumption

- 10 mA typical active current

Space Efficien Packaging

- 8-pin SOIC 208-mil
- 8-pad WSON 6x5-mm
- SOP16 (300mil)
- Contact Zetta for KGD and other options

Note: 1.Please contact Zetta for details.

GENERAL DESCRIPTION

The ZD25Q64 (64M-bit) Serial Flash memory provides a storage solution for systems with limited space, pins and power. The ZD25Q64 series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The device operates on a single 2.7V to 3.6V power supply with current consumption as low as 10mA active. All devices are offered in space- saving packages.

The ZD25Q64 support the standard Serial Peripheral Interface (SPI), as well as Dual/Quad I/O SPI: Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 108MHz are supported allowing equivalent clock rates of 216MHz (108MHz x 2) for Dual I/O and 432MHz (108MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O instructions. These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories.

A Hold pin, Write Protect pin and programmable write protection, with top or bottom array control, provide further control flexibility.

1. ORDERING INFORMATION

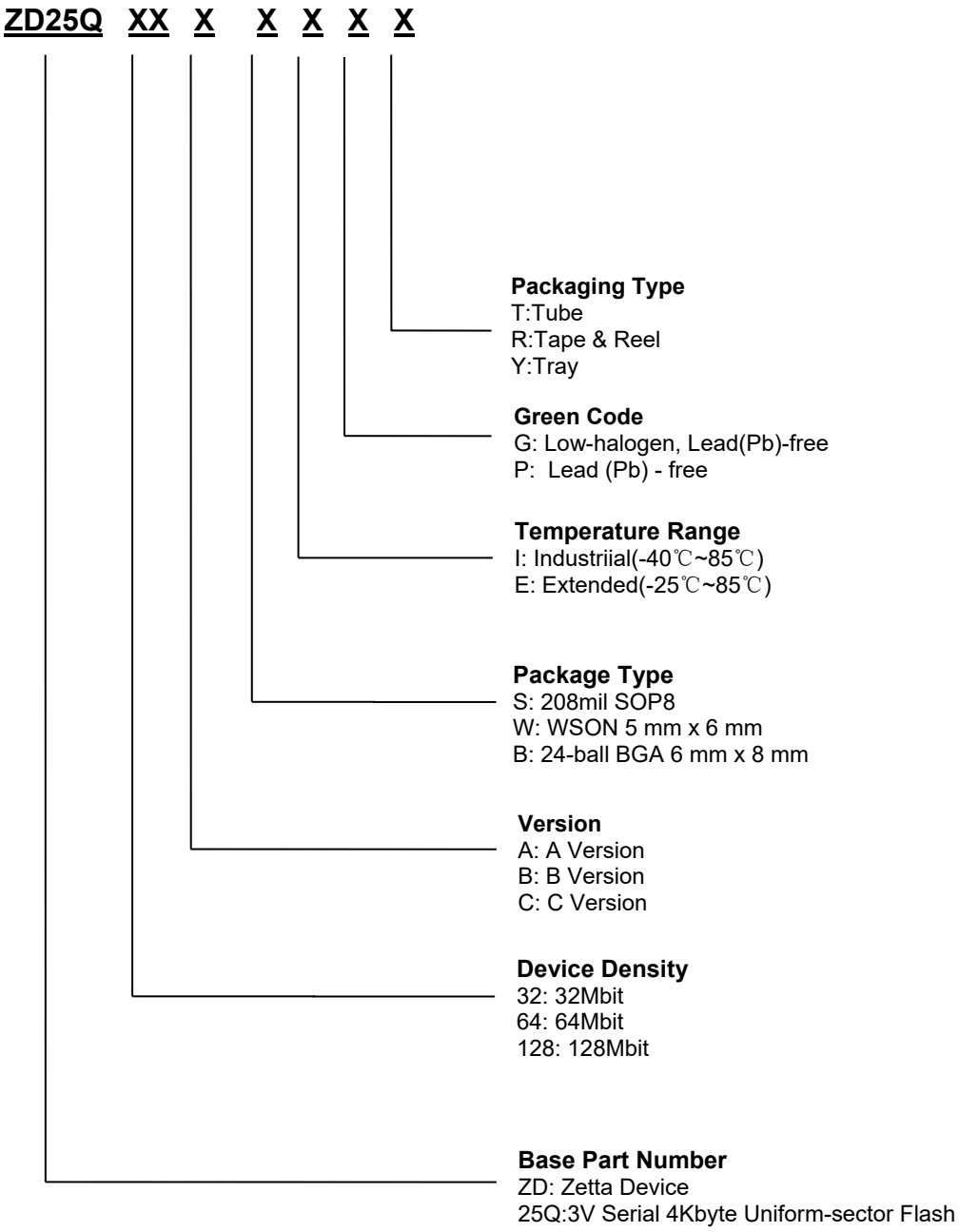


Figure 1, Ordering Information

2. BLOCK DIAGRAM

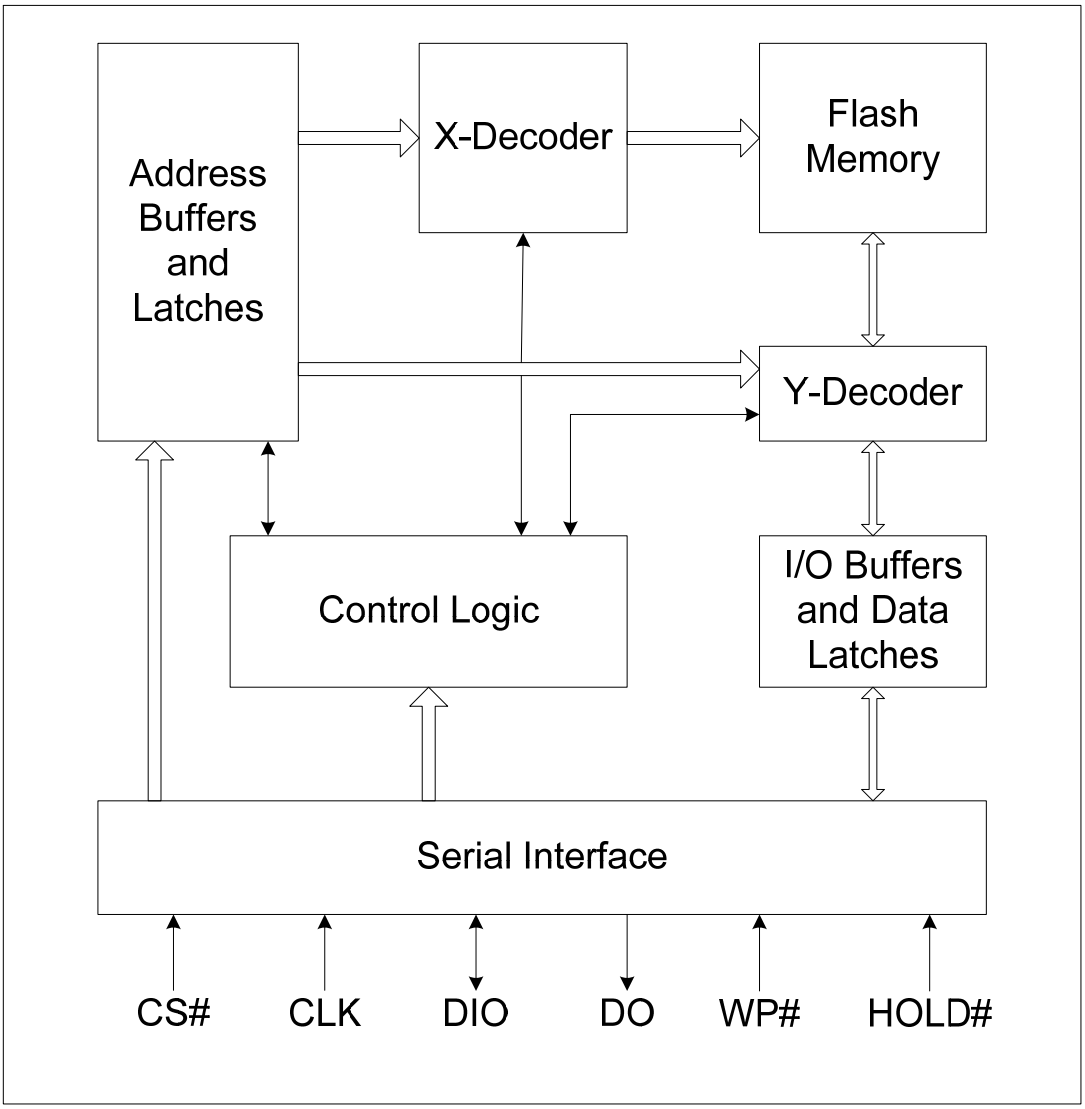


Figure 2, Block Diagram

3. CONNECTION DIAGRAMS

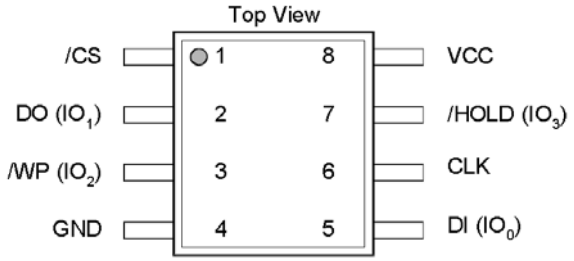


Figure 3.1, 8-pin SOP (208mil)

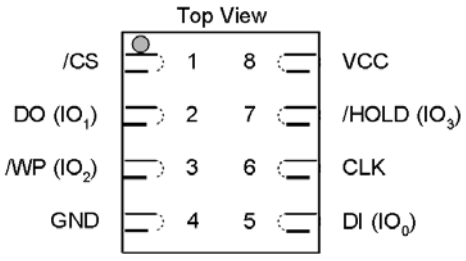


Figure 3.2, 8-Contact 6 x 5 mm WSON

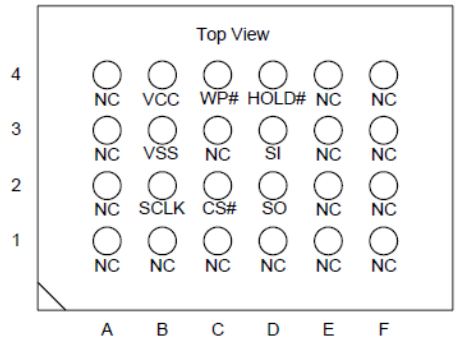


Figure 3.3, 24-BALL TFBGA

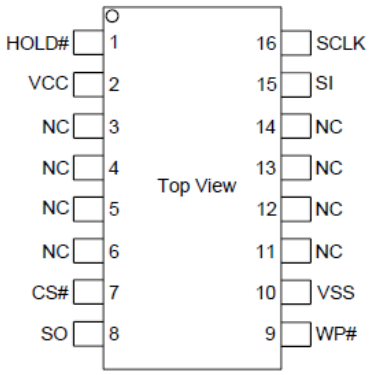


Figure 3.4, 16-LEAD SOP

4. SIGNAL DESCRIPTIONS

Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)
The ZD25Q64 supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK. Dual/Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. When use Quad Output instructions, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

Serial Clock (CLK)
The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Mode")

Chip Select (CS#)
The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high, the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low, the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up and power-down. If needed a pull-up resister on /CS can be used to accomplish this.

Write Protect (WP#)
The Write Protect (/WP) pin can be used to prevent the Status Registers from being written. Used in Conjunction with the Status Register's Block Protect (CMP, SEC, TB, BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion as small as a 4KB sector or the entire memory array can be hardware protected. The /WP pin is active low.

Table1, Pin Descriptions

Symbol	Pin Name
/CS	Chip Select Input
DO (IO1)	Data Output (Data Input Output 1)*1
/WP (IO2)	Write Protect Input (Data Input Output 2)*2
GND	Ground
DI (IO0)	Data Input (Data Input Output 0)*1
CLK	Serial Clock Input
/HOLD (IO3)	Hold Input (Data Input Output 3)*2

*1 IO0 and IO1 are used for Standard and Dual SPI instructions

*2 IO3 are used for Quad SPI instructions

5. MEMORY ORGANIZATIONS

The memory is organized as:
- 8,388,608bytes
- Uniform Sector Architecture
  128 blocks of 64-Kbyte
  2,048 sectors of 4-Kbyte
  32,768 pages (256 bytes each)

Each page can be individually programmed (bits are programmed from 1 to 0). The device is Sector, Block or Chip Erasable but not Page Erasable.

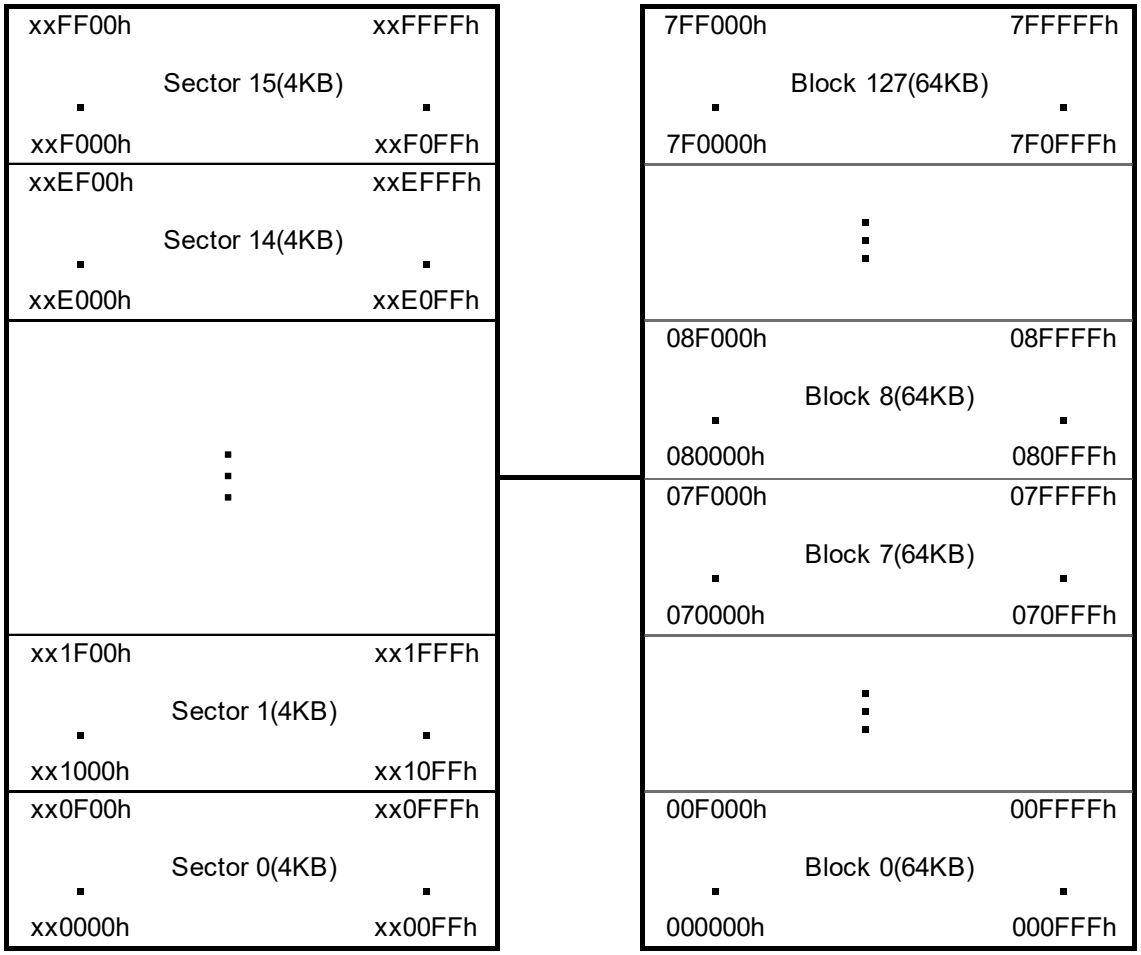


Figure 4, Memory Organization

6. FUNCTION DESCRIPTION

Standard SPI Instructions

The ZD25Q64 is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

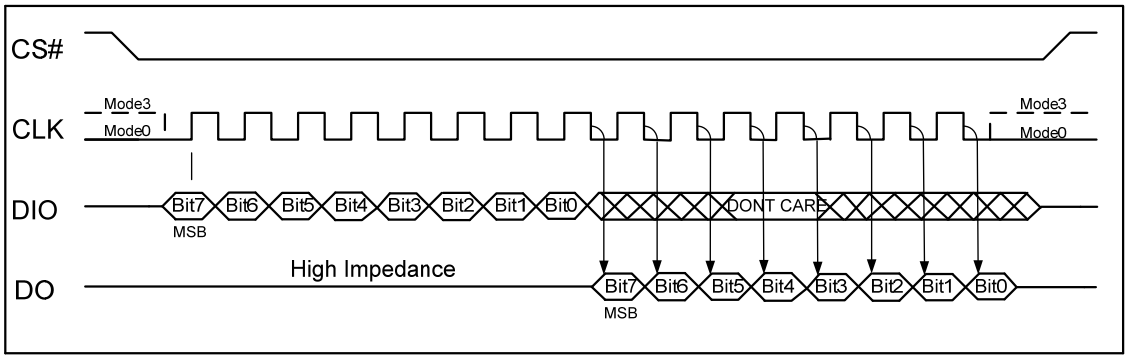


Figure 5, SPI Modes

Dual SPI

The ZD25Q64 supports Dual SPI operation when using the “Dual Output Fast Read” (3BH) and “Dual I/O Fast Read” (BBH) commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1. Dual SPI commands require the non-volatile Dual Enable bit (DE) in Nonvolatile Configuration Register to be set.

Quad SPI

The ZD25Q64 supports Quad SPI operation when using the “Quad Output Fast Read” (6BH), “Quad I/O Fast Read” (EBH) and “Quad Page Program” (32H) commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and WP# and HOLD# pins become IO2 and IO3. Quad SPI commands require the non-volatile Quad Enable bit (QE) in Nonvolatile Configuration Register to be set.

Hold

The HOLD# function is only available when QE=0, If QE=1, The HOLD# functions is disabled, the pin acts as dedicated data I/O pin.

The HOLD# signal goes low to stop any serial communications with the device, but doesn’t stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD, need CS# keep low, and starts on falling edge of the HOLD# signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK being low). The HOLD condition ends on rising edge of HOLD# signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK being low).

The SO is high impedance, both SI and SCLK don’t care during the HOLD operation, if CS# drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and then CS# must be at low.

7. STATUS REGISTER AND CONFIGURATION REGISTERS

Status Register

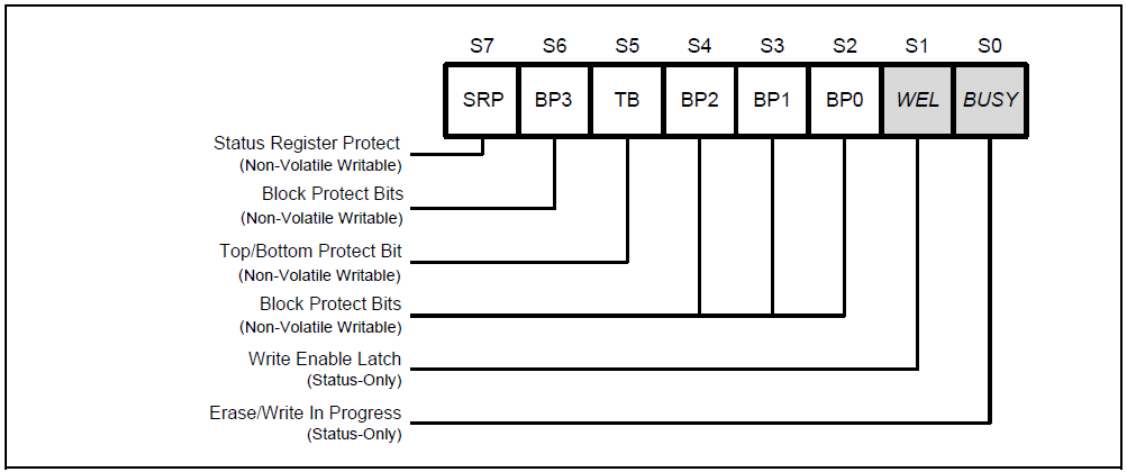


Figure 6, Status Register

- **BUSY**
  BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction. During this time the device will ignore further instructions except for the Read Status Register instruction (see tW, tPP, tSE, tBE, and tCE in AC Characteristics). When the program, erase or write status register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

- **Write Enable Latch (WEL)**
  Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to a 1 after executing a Write Enable Instruction. The WEL status bit is cleared to a 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Sector Erase, Block Erase, Chip Erase and Write Status Register.

- **Block Protect Bits (BP3, BP2, BP1, BP0)**
  Block Protect Bits (BP3, BP2, BP1, BP0) are non-volatile read/write bits in the status register (S6, S4, S3 and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see tW in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected. The Block Protect bits can not be written to if the Status Register Protect (SRP) bit is set to 1 and the Write Protect (/WP) pin is low.

- **Top/Bottom Block Protect (TB)**
  The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP3, BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP and WEL bits.

- **Status Register Protect (SRP)**
  The Status Register Protect bits (SRP) are non-volatile read/write bits in the status register (S7). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down.

Nonvolatile Configuration Register

Bit	Name	Settings	Description	Notes
15:12	Number of dummy clock cycles	0000 (identical to 1111) 0001 0010 . . 1101 1110 1111	Sets the number of dummy clock cycles subsequent to all FAST READ commands. The default setting targets the maximum allowed frequency and guarantees backward compatibility.	2,3
11:9	XIP mode at power-on reset	000 = XIP: Fast Read 001 = XIP: Dual Output Fast Read 010 = XIP: Dual I/O Fast Read 011 = XIP: Quad Output Fast Read 100 = XIP: Quad I/O Fast Read 101 = Reserved 110 = Reserved 111 = Disabled (Default)	Enables the device to operate in the selected XIP mode immediately after power-on reset.	
8:6	Output driver strength	000 = Reserved 001 = 90 Ohms 010 = 60 Ohms 011 = 45 Ohms 100 = Reserved 101 = 20 Ohms 110 = 15 Ohms 111 = 30 (Default)	Optimizes impedance at VCC/2 output voltage.	
5	Reserved	X	Don't Care.	
4	Reset/hold	0 = Disabled 1 = Enabled (Default)	Enables or disables hold or reset.	
3	QE	0 = Enabled 1 = Disabled (Default)	Enables or disables quad I/O protocol.	4
2	DE	0 = Enabled 1 = Disabled (Default)	Enables or disables dual I/O protocol.	4
1:0	Reserved	X	Don't Care.	

Notes:

1. Settings determine device memory configuration after power-on. The device ships from the factory with all bits erased to 1 (FFFFh). The register is read from or written to by READ NONVOLATILE CONFIGURATION REGISTER or WRITE NONVOLATILE CONFIGURATION REGISTER commands, respectively.
2. The 0000 and 1111 settings are identical in that they both define the default state, which is the maximum frequency of fc = 108 MHz. This ensures backward compatibility.
3. If the number of dummy clock cycles is insufficient for the operating frequency, the memory reads wrong data. The number of cycles must be set according to and sufficient for the clock frequency, which varies by the type of FAST READ command, as shown in the Supported Clock Frequencies table.
4. If bits 2 and 3 are both set to 0, the device operates in quad I/O. When bits 2 or 3 are reset to 0, the device operates in dual I/O or quad I/O respectively, after the next poweron.

Volatile Configuration Register

Bit	Name	Settings	Description	Notes
7:4	Number of dummy clock cycles	0000 (identical to 1111) 0001 0010 . . 1101 1110 1111	Sets the number of dummy clock cycles subsequent to all FAST READ commands. The default setting targets the maximum allowed frequency and guarantees backward compatibility.	2,3
3	XIP	0 = Enable 1 = Disable (default)	Enables or disables XIP. For device part numbers with the feature digit equal to 2 or 4, this bit is always "Don't Care," so the device operates in XIP mode without setting this bit.	
2	Reserved	X	0b = Fixed value.	
1:0	Wrap	00 = 16-byte boundary aligned 01 = 32-byte boundary aligned 10 = 64-byte boundary aligned 11 = sequential (default)	16-byte wrap: Output data wraps within an aligned 16-byte boundary starting from the 3-byte address issued after the command code. 32-byte wrap: Output data wraps within an aligned 32-byte boundary starting from the 3-byte address issued after the command code. 64-byte wrap: Output data wraps within an aligned 64-byte boundary starting from the 3-byte address issued after the command code. Continuous reading (default): All bytes are read sequentially.	4

Notes:

1. Settings determine the device memory configuration upon a change of those settings by the WRITE VOLATILE CONFIGURATION REGISTER command. The register is read from or written to by READ VOLATILE CONFIGURATION REGISTER or WRITE VOLATILE CONFIGURATION REGISTER commands respectively.
2. The 0000 and 1111 settings are identical in that they both define the default state, which is the maximum frequency of fc = 108 MHz. This ensures backward compatibility.
3. If the number of dummy clock cycles is insufficient for the operating frequency, the memory reads wrong data. The number of cycles must be set according to and be sufficient for the clock frequency, which varies by the type of FAST READ command, as shown in the Supported Clock Frequencies table.
4. See the Sequence of Bytes During Wrap table.

Flag Status Register

Bit	Name	Settings	Description	Notes
7	Program or erase controller	0 = Busy 1 = Ready	**Status bit:** Indicates whether a PROGRAM, ERASE, WRITE STATUS REGISTER, or WRITE NONVOLATILE CONFIGURATION command cycle is in progress.	2,3
6	Erase suspend	0 = Not in effect 1 = In effect	**Status bit:** Indicates whether an ERASE operation has been or is going to be suspended.	3
5	Erase	0 = Clear 1 = Failure or protection error	**Error bit:** Indicates whether an ERASE operation has succeeded or failed.	4,5
4	Program	0 = Clear 1 = Failure or protection error	**Error bit:** Indicates whether a PROGRAM operation has succeeded or failed. Moreover, indicates an attempt to program a 0 to a 1 when VPP = VPPH and the data pattern is a multiple of 64 bits.	4,5
3	VPP	0 = Enabled 1 = Disabled (Default)	**Error bit:** Indicates an invalid voltage on VPP during a PROGRAM or ERASE operation.	4,5
2	Program suspend	0 = Not in effect 1 = In effect	**Status bit:** Indicates whether a PROGRAM operation has been or is going to be suspended.	3
1	Protection	0 = Clear 1 = Failure or protection error	**Error bit:** Indicates whether an ERASE or a PROGRAM operation has attempted to modify the protected array sector. Moreover, indicates whether a PROGRAM operation has attempted to access the locked OTP space.	4,5
0	Reserved	Reserved	Reserved	

Supported Clock Frequencies

Number of Dummy Clock Cycles	FAST READ	DUAL OUTPUT FAST READ	DUAL I/O FAST READ	QUAD OUTPUT FAST READ
1	54	50	39	43
2	95	85	59	56
3	105	95	75	70
4	108	105	88	83
5	108	108	94	94
6	108	108	105	105
7	108	108	108	108
8	108	108	108	108
9	108	108	108	108
10	108	108	108	108

- **ZD25Q64 Status Register Memory Protection (Upper Area)**

Status Register Content					Memory Content	
TB	**BP3**	**BP2**	**BP1**	**BP0**	**PROTECTED AREA**	**UNPROTECTED AREA**
0	0	0	0	0	None	All Blocks
0	0	0	0	1	Upper 128th	Blocks (0 to 126)
0	0	0	1	0	Upper 64th	Blocks (0 to 125)
0	0	0	1	1	Upper 32nd	Blocks (0 to 123)
0	0	1	0	0	Upper 16th	Blocks (0 to119)
0	0	1	0	1	Upper 8th	Blocks (0 to 111)
0	0	1	1	0	Upper quarter	Blocks (0 to 95)
0	0	1	1	1	Upper half	Blocks (0 to 63)
0	1	0	0	0	All blocks	None
0	1	0	0	1	All blocks	None
0	1	0	1	0	All blocks	None
0	1	0	1	1	All blocks	None
0	1	1	0	0	All blocks	None
0	1	1	0	1	All blocks	None
0	1	1	1	0	All blocks	None
0	1	1	1	1	All blocks	None

Note:
1. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

- **ZD25Q64 Status Register Memory Protection (Lower Area)**

Status Register Content					Memory Content	
TB	BP3	BP2	BP1	BP0	PROTECTED AREA	UNPROTECTED AREA
1	0	0	0	0	None	All Blocks
1	0	0	0	1	Lower 128th	Blocks (1 to 127)
1	0	0	1	0	Lower 64th	Blocks (2 to 127)
1	0	0	1	1	Lower 32nd	Blocks (4 to 127)
1	0	1	0	0	Lower 16th	Blocks (8 to 127)
1	0	1	0	1	Lower 8th	Blocks (16 to 127)
1	0	1	1	0	Lower quarter	Blocks (32 to 127)
1	0	1	1	1	Lower half	Blocks (64 to 127)
1	1	0	0	0	All blocks	None
1	1	0	0	1	All blocks	None
1	1	0	1	0	All blocks	None
1	1	0	1	1	All blocks	None
1	1	1	0	0	All blocks	None
1	1	1	0	1	All blocks	None
1	1	1	1	0	All blocks	None
1	1	1	1	1	All blocks	None

Note:

1. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

8 INSTRUCTIONS

The instruction set of the ZD25Q64 consists of fifteen basic instructions that are fully controlled through the SPI bus (see Instruction Set table). Instructions are initiated with the falling edge of Chip Select (CS#). The first byte of data clocked into the DIO input provides the instruction code. Data on the DIO input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge CS#. Clock relative timing diagrams for each instruction are included in figures 7 through 24. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (CS driven high after a full 8-bits have been clocked) otherwise the instruction will be terminated. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

Table 4, Instruction Set(1)

INSTRUCTION NAME	BYTE1 CODE	BYTE2	BYTE3	BYTE4	BYTE5	BYTE6	BYTE7	N-BYTES
Write Enable	06h							
write Disable	04h							
Read Status Register	05h	(S7-S0)(2)						
Read Nonvolatile Configuration Register	B5h	(D7-D0)(2)	(D15-D8)(2)					
Read Volatile Configuration Register	85h	(D7-D0)(2)						
Write Status Register(4)	01h	S7-S0(4)						
Write Nonvolatile Configuration Register	B1h	(D7-D0)	(D15-D8)					
Write Volatile Configuration Register	81h	(D7-D0)						
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	(Next byte)	Continuous
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(D7-D0)	(Next byte) continuous
Fast Read Dual Output	3Bh	A23-A16	A15-A8	A7-A0	dummy	I/O= (D6,D4,D2,D0) O= (D7,D5,D3,D1)	(One byte per 4 clocks, continuous)	
Dual I/O Fast Read	BBh	A23-A16	A15-A8	A7-A0	dummy	I/O= (D6,D4,D2,D0) O= (D7,D5,D3,D1)	(One byte per 4 clocks, continuous)	
Fast Read Quad Output	6Bh	A23-A16	A15-A8	A7-A0	dummy	IO0 = (D4, D0) IO1 = (D5, D1) IO2 = (D6, D2) IO3 = (D7, D3)	(One byte per 2 clocks, continuous)	
Quad I/O Fast Read	EBh	A23-A16	A15-A8	A7-A0	M7-M0	dummy	dummy	(D7-D0)
Page Program	02h	A23-A16	A15-A8	A7-A0	(D7-D0)(3)	(Next byte)	Up to 256	
Quad Page Program	32h	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	Up to 256	
Block Erase(64KB)	D8h	A23-A16	A15-A8	A7-A0				

Sector Erase(4KB)	20h	A23-A16	A15-A8	A7-A0				
Chip Erase	C7h/60 h							
Program/Erase Suspend	75h							
Program/Erase Resume	7Ah							
JEDEC ID	9Fh	(MID7-MID0)	(ID15-ID8) Memory Type	(ID7-ID0) Capacity				
Read Serial Flash Discoverable Parameter(4)	5Ah	A23-A16	A15-A8	A7-A0	dummy	D7-D0		
Program OTP array(4)	42h	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0	continuous	
Read OTP array(4)	4Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	continuous	

Notes:
1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis “( )” indicate data output from the device on either 1, 2 or 4 IO pins.
2. The Status Register contents and Device ID will repeat continuously until /CS terminates the instruction.
3. At least one byte of data input is required for Page Program, Quad Page Program, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.
4. This feature is available upon special order. Please contact Zetta for details.

Table 5, Manufacturer and Device Identification

OP Code	(MID7-MID0)	(ID15-ID0)	(ID7-ID0)
9Fh	BAh	BA17h	

8.1 Write Enable (06h)

The Write Enable instruction (Figure 7) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Sector Erase, Block Erase, Chip Erase and Write Status Register instruction. The Write Enable instruction is entered by driving CS# low, shifting the instruction code "06h" into the Data Input (DI) pin on the rising edge of CLK, and then driving CS# high.

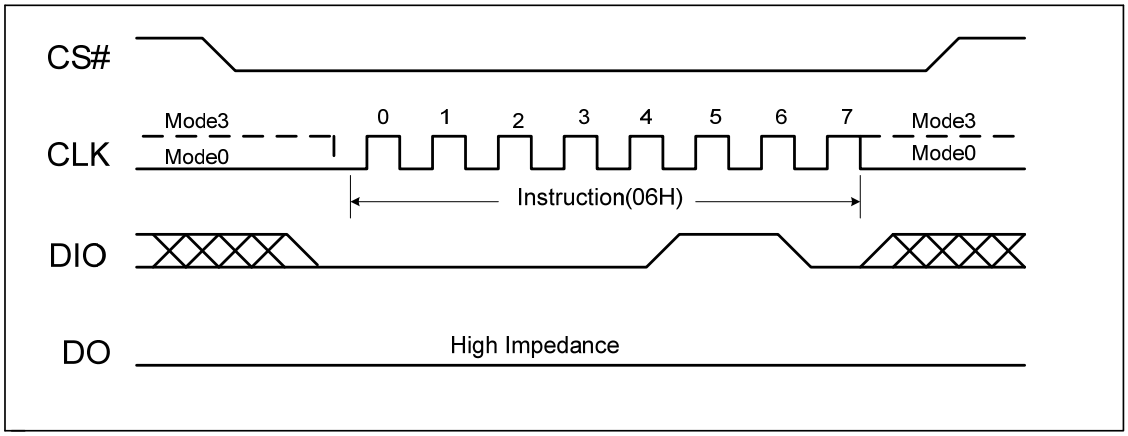


Figure 7, Write Enable Instruction Sequence Diagram

8.2 Write Disable (04h)

The Write Disable instruction (Figure 8) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving CS# low, shifting the instruction code "04h" into the DIO pin and then driving CS# high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase instructions.

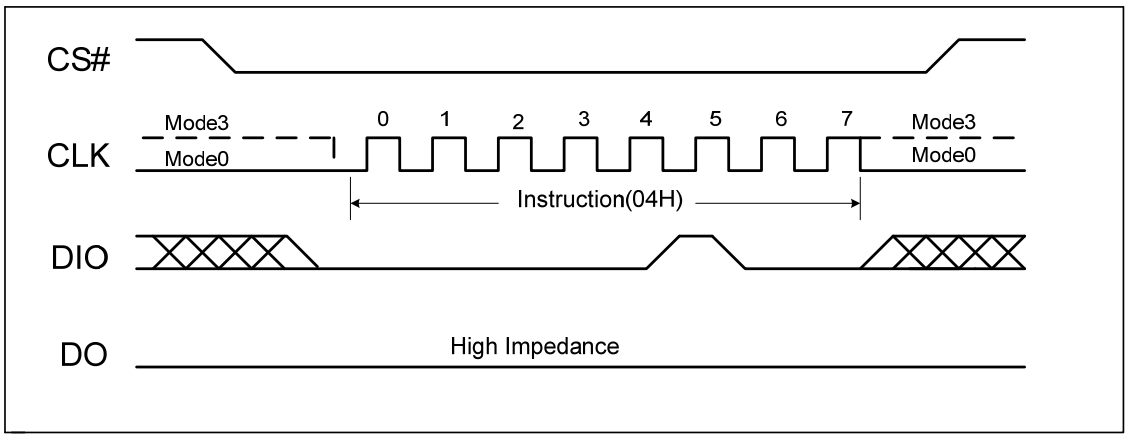
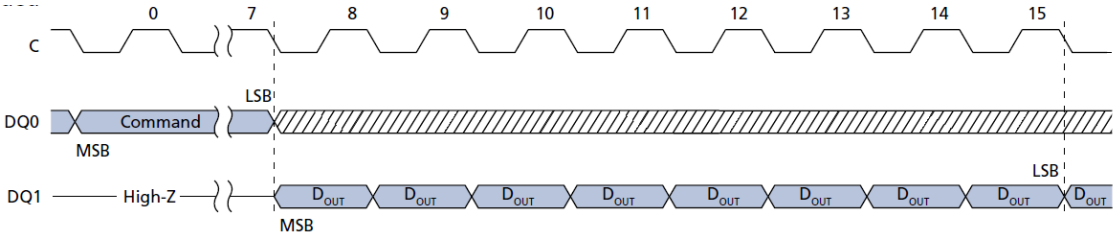


Figure 8, Write Disable Instruction Sequence Diagram

8.3 Read Register (05H or B5H or 85H)

The Read Register command is for reading the Register. The Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write in Progress (WIP) bit before sending a new command to the device.



Note:

1. A READ NONVOLATILE CONFIGURATION REGISTER operation will output data starting from the least significant byte.

Figure 9, Read Register Instruction Sequence Diagram

8.4 Write Register (01H or B1H or 81H)

8.4.1 WRITE STATUS REGISTER Command

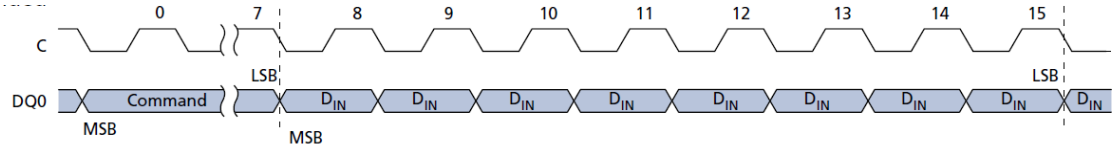
To issue a WRITE STATUS REGISTER command, the WRITE ENABLE command must be executed to set the write enable latch bit to 1. S# is driven LOW and held LOW until the eighth bit of the last data byte has been latched in, after which it must be driven HIGH. For extended SPI protocol, the command code is input on DQ0, followed by the data bytes. This command is used to write new values to status register bits 7:2, enabling software data protection. The status register can also be combined with the W#/VPP signal to provide hardware data protection. The WRITE STATUS REGISTER command has no effect on status register bits 1:0. When the operation is in progress, the write in progress bit is set to 1. The write enable latch bit is cleared to 0, whether the operation is successful or not. The status register and flag status register can be polled for the operation status. When the operation completes, the write in progress bit is cleared to 0, whether the operation is successful or not.

8.4.2 WRITE NONVOLATILE CONFIGURATION REGISTER Command

To execute the WRITE NONVOLATILE CONFIGURATION REGISTER command, the WRITE ENABLE command must be executed to set the write enable latch bit to 1. S# is driven LOW and held LOW until the 16th bit of the last data byte has been latched in, after which it must be driven HIGH. For extended SPI protocol, the command code is input on DQ0, followed by two data bytes.
When the operation is in progress, the write in progress bit is set to 1. The write enable latch bit is cleared to 0, whether the operation is successful or not. The status register and flag status register can be polled for the operation status. When the operation completes, the write in progress bit is cleared to 0.

8.4.3 WRITE VOLATILE CONFIGURATION REGISTER Command

To execute a WRITE VOLATILE CONFIGURATION REGISTER command, the WRITE ENABLE command must be executed to set the write enable latch bit to 1. S# is driven LOW and held LOW until the eighth bit of the last data byte has been latched in, after which it must be driven HIGH. For extended SPI protocol, the command code is input on DQ0, followed by the data bytes.



Note:

1. A WRITE NONVOLATILE CONFIGURATION REGISTER operation requires data being sent starting from least significant byte.

Figure 10, Write Register Instruction Sequence Diagram

8.5 Read Data (Read) (03h)

The Read Data instruction allows one more data bytes to be sequentially read from the memory. The instruction is initiated by driving the CS# pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23-A0) into the DIO pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving CS# high.

The Read Data instruction sequence is shown in figure 11. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of fR (see AC Electrical Characteristics).

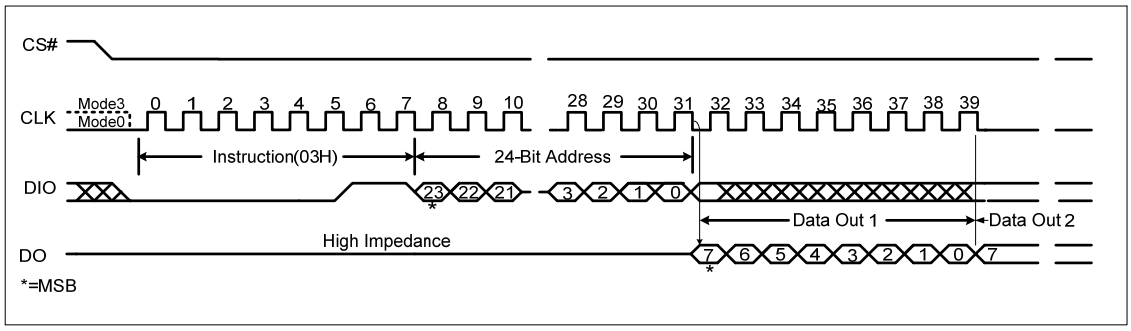


Figure 11. Read Data Instruction Sequence Diagram

8.6 Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in figure 12. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DIO pin is a “don’t care”.

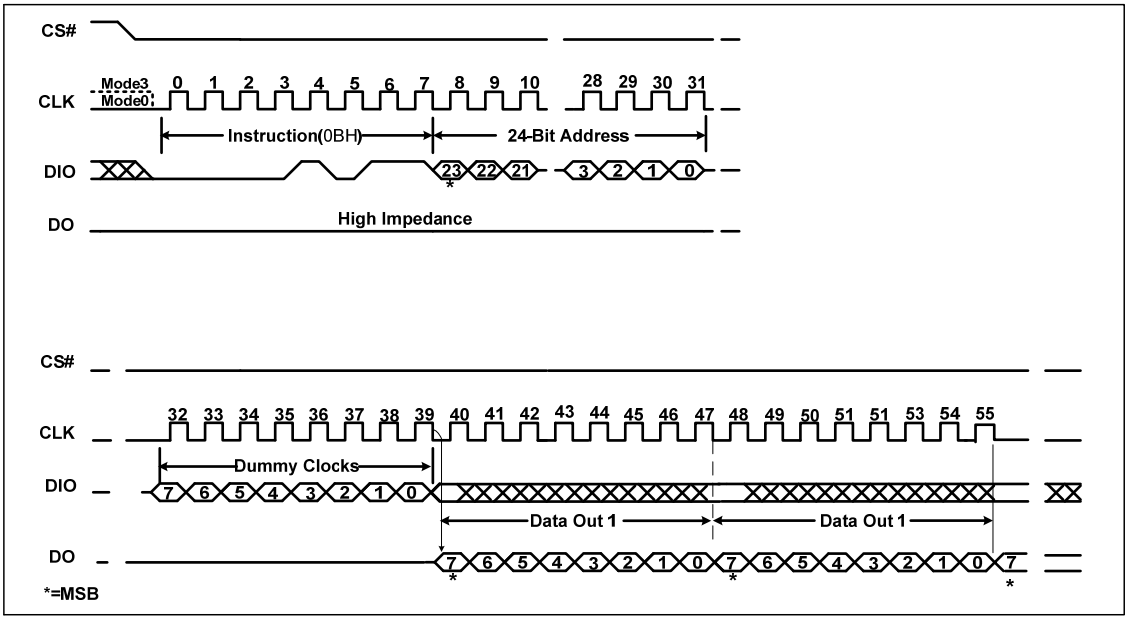


Figure 12, Fast Read Instruction Sequence Diagram

8.7 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins, DO and DIO, instead of just DO. This allows data to be transferred from the ZD25Q64 at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in figure 13. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the DIO pin should be high-impedance prior to the falling edge of the first data out clock.

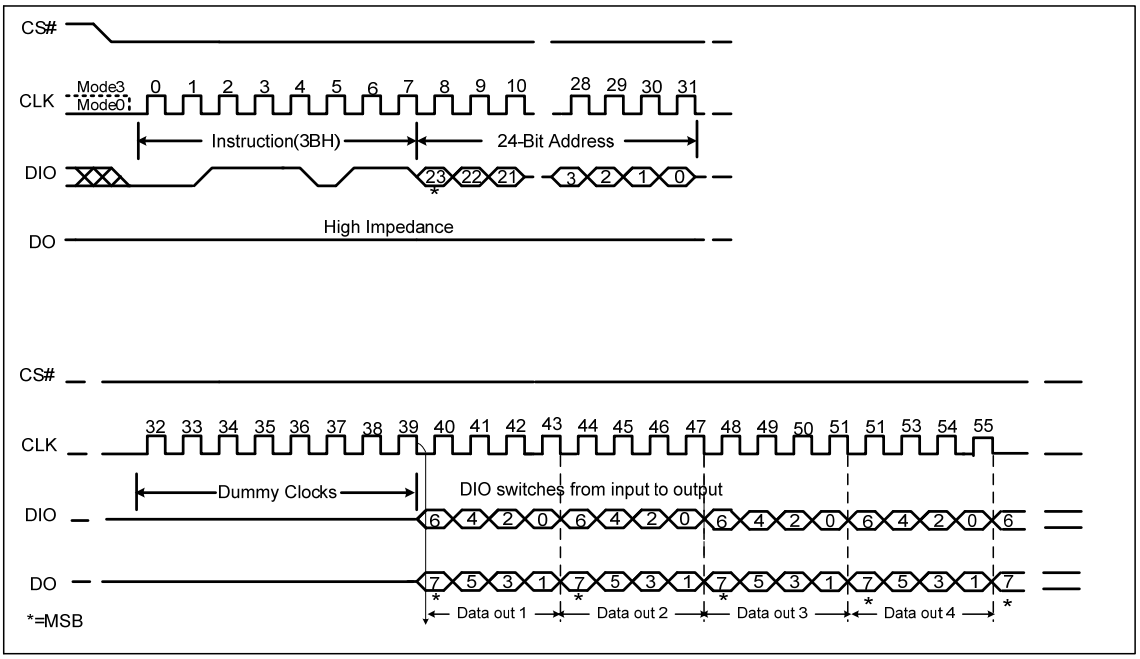


Figure 13, Fast Read Dual Output Instruction Sequence Diagram

8.8 Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, IO_0, IO_1, IO_2, and IO_3. The Fast Read Quad Output Instruction allows data to be transferred from the ZD25Q at four times the rate of standard SPI devices. The Fast Read Quad Output instruction can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 14. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

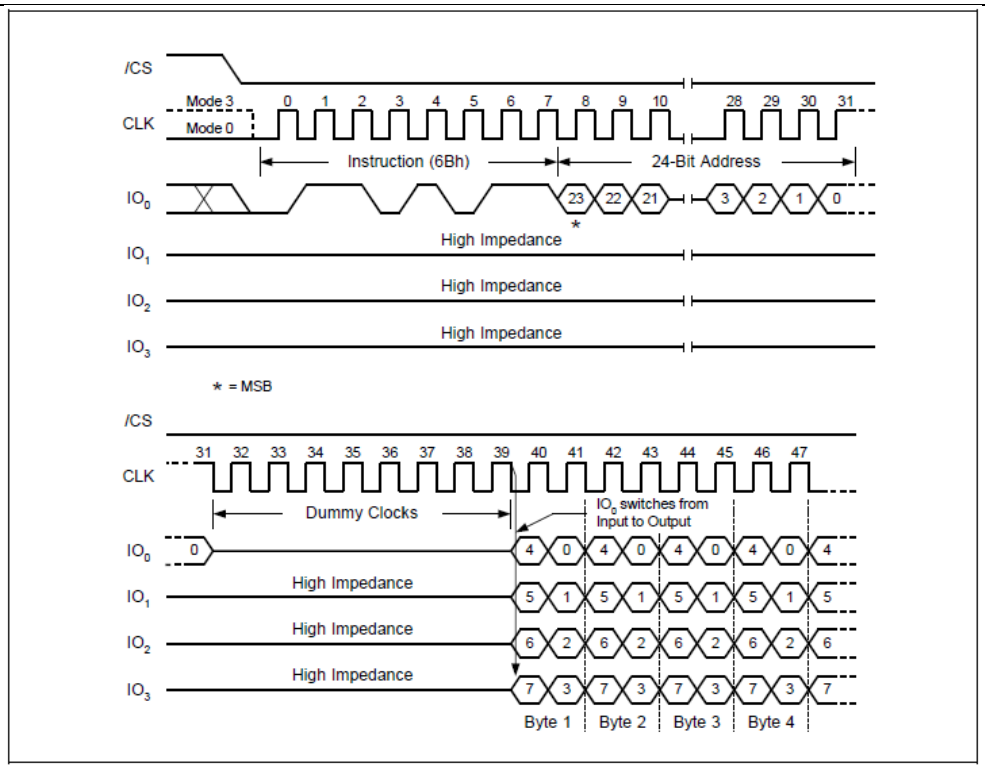


Figure 14, Fast Read Quad Output Instruction Sequence Diagram

8.9 Fast Read Dual I/O (BBh)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3-byte address (A23-0) 2-bit per clock by SI and SO, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in followed Figure15. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Dual Enable bit (DE) of NONVOLATILE CONFIGURATION REGISTER must be set to enable the Fast Read Dual I/O Instruction.

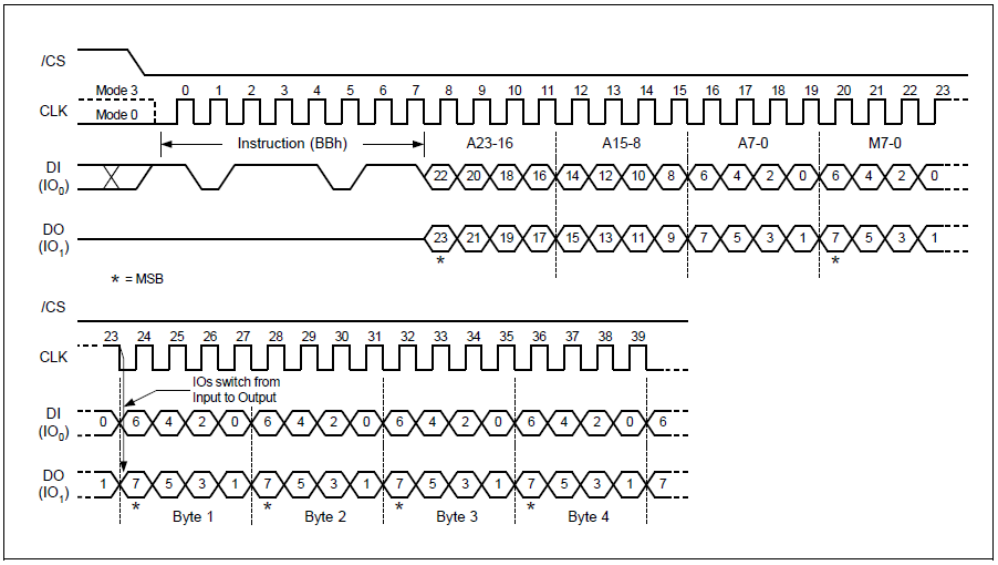


Figure 15, Dual I/O Fast Read Sequence Diagram

8.10 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO0, IO1, IO2 and IO3 and four Dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of NONVOLATILE CONFIGURATION REGISTER must be set to enable the Fast Read Quad I/O Instruction.

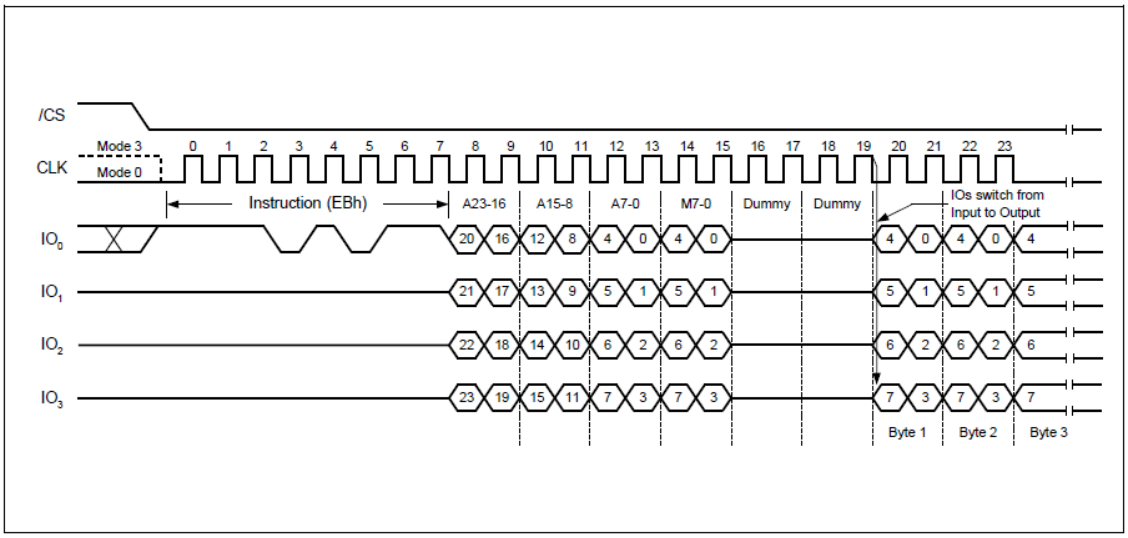


Figure 16, Quad I/O Fast Read Sequence Diagram

8.11 Page Program (PP) (02h)

The Page Program instruction allows up to 256 bytes of data to be programmed at previously erased to all 1s (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low then shifting the instruction code “02h” followed by a 24-bit address (A23-A0) and at least one data byte, into the DIO pin. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in figure 17.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceed the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks can not exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After CS# is driven high, the self-timed Page Program instruction will commence for a time duration of tpp (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

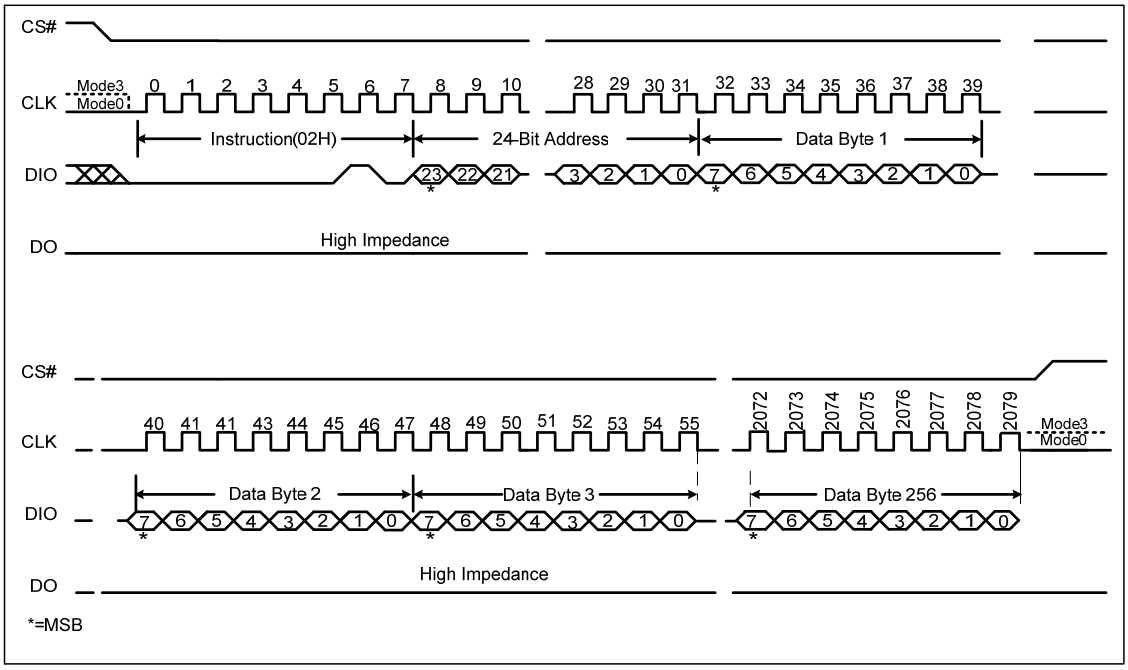


Figure 17, Page Program Instruction Sequence Diagram

8.12 Quad Input Page Program (32h)

The Quad Page Program instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: IO0, IO1, IO2, and IO3. The Quad Page Program can improve performance for PROM Programmer and applications that have slow clock speeds <5MHz. Systems with faster clock speed will not realize much benefit for the Quad Page Program instruction since the inherent page program time is much greater than the time it take to clock-in the data.

To use Quad Page Program the Quad Enable in NONVOLATILE CONFIGURATION REGISTER must be set (QE=1). A Write Enable instruction must be executed before the device will accept the Quad Page Program instruction (Status Register, WEL=1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “32h” followed by a 24-bit address (A23-A0) and at least one data byte, into the IO pins. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Page Program are identical to standard Page Program. The Quad Page Program instruction sequence is shown in Figure 18.

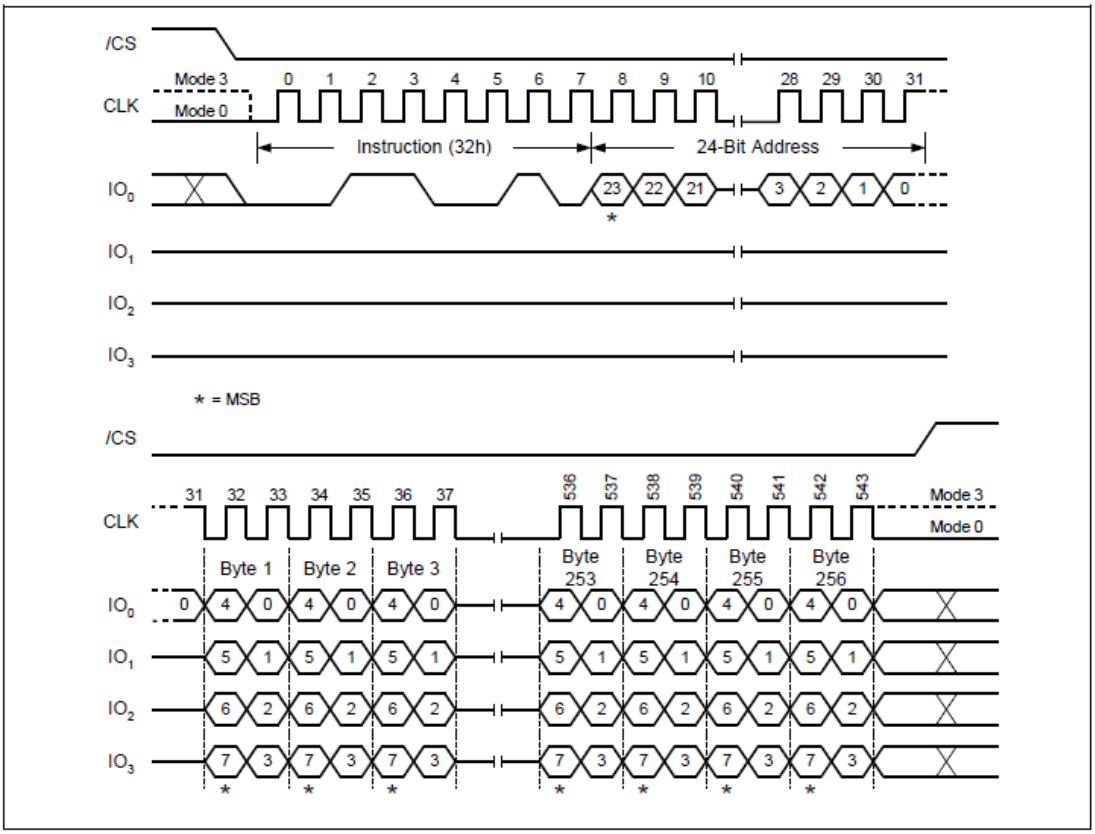


Figure 18, Quad Page Program Sequence Diagram

8.13 Sector Erase (SE) (20h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “20h” followed a 24-bit sector address (A23-A0). The Sector Erase instruction sequence is shown in figure 19.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After CS# is driven high, the self-timed Sector Erase instruction will commence for a time duration of tSE (See AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

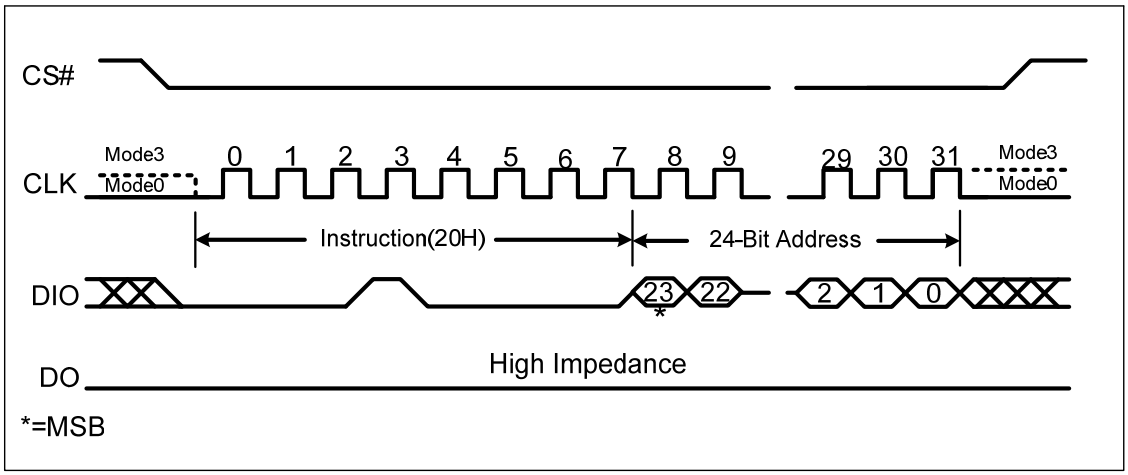


Figure 19, Sector Erase Instruction Sequence Diagram

8.14 Block Erase (BE) (D8h)

The Block Erase instruction sets all memory within a specified block (64K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code "D8h" followed a 24-bit block address (A23-A0). The Block Erase instruction sequence is shown in figure 20.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After CS# is driven high, the self-timed Block Erase instruction will commence for a time duration of tBE (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

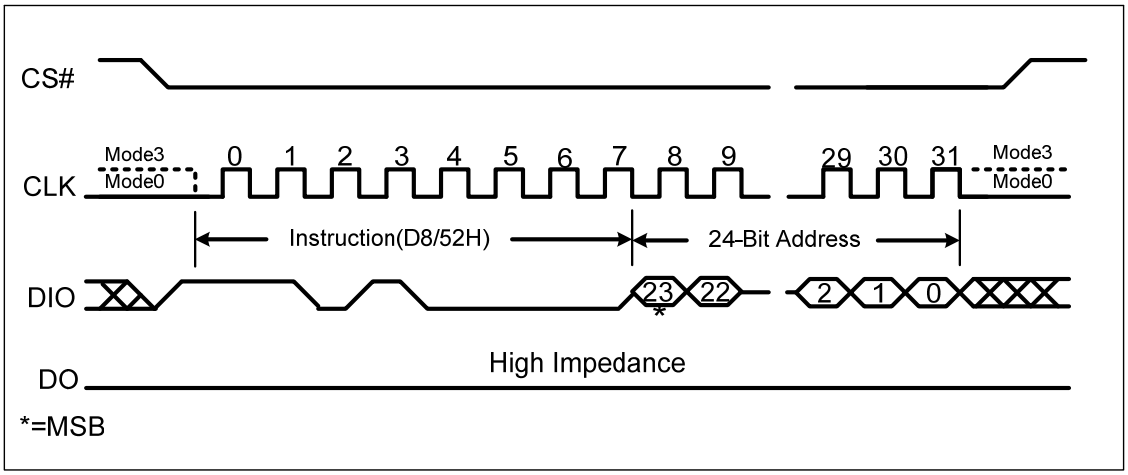


Figure 20. Block Erase Instruction Sequence Diagram

8.15 Chip Erase (CE) (C7h or 60h)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in figure 21.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After CS# is driven high, the self-timed Chip Erase instruction will commence for a time duration of tCE (See AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any page is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

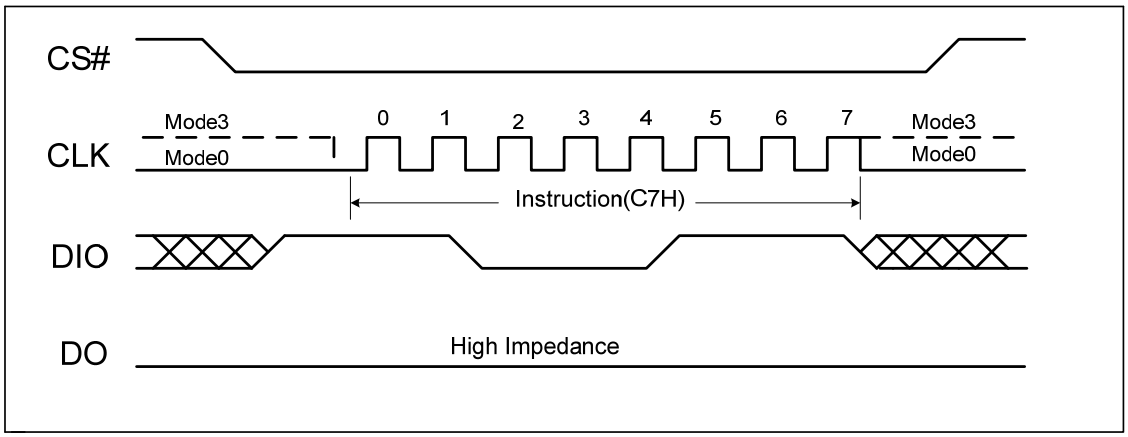


Figure 21, Chip Erase Instruction Sequence Diagram

8.16 Read Identification (RDID) (9Fh)

For compatibility reasons, the ZD25Q64 provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003.

The instruction is initiated by driving the CS# pin low and shifting the instruction code “9Fh”. The JEDEC assigned Manufacturer ID byte for Zetta Device and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in figure 22. For memory type and capacity values refer to Manufacturer and Device Identification table.

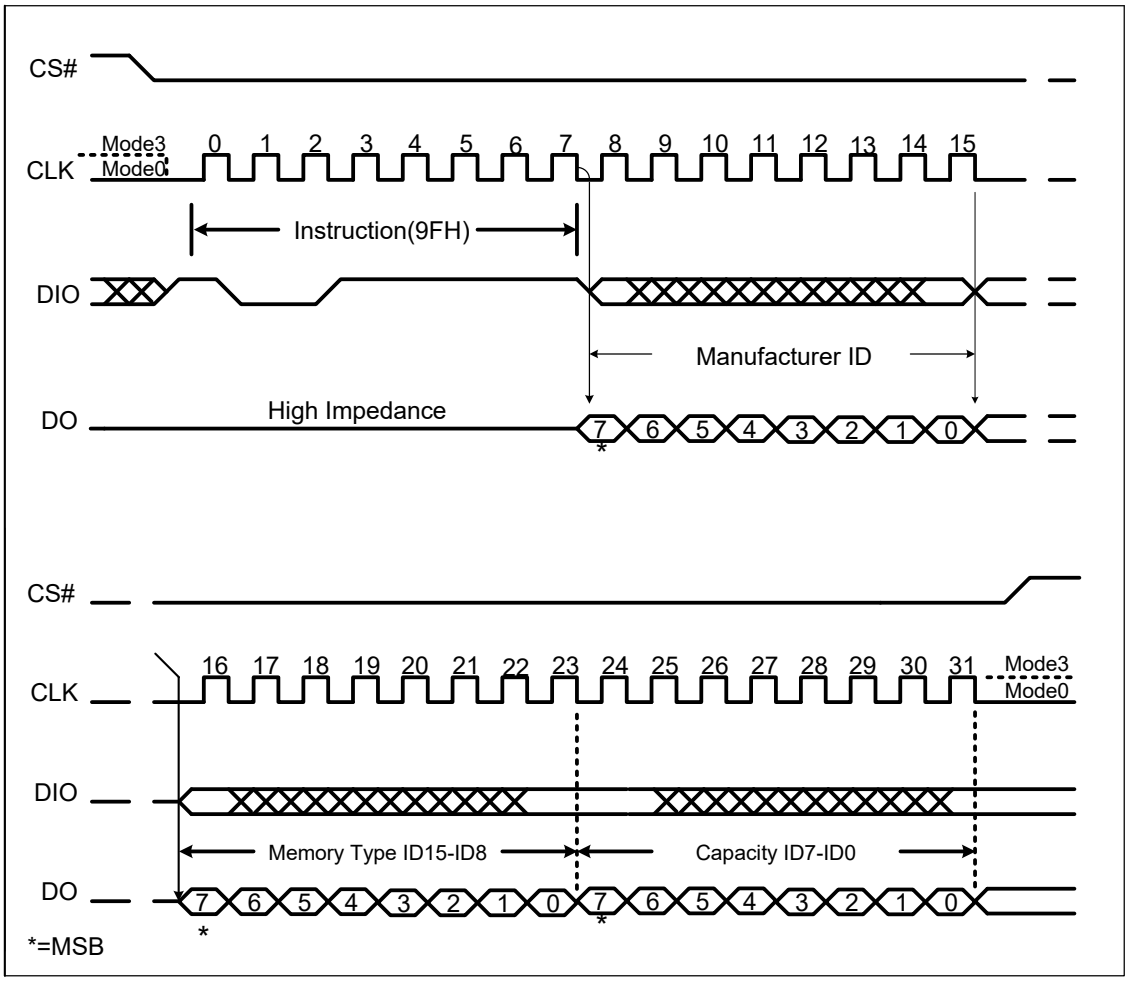


Figure 22, Read JEDEC ID instruction Sequence Diagram

8.17 Program/Erase Suspend (PES) (75h)

To initiate the PROGRAM/ERASE SUSPEND command, S# is driven LOW. The command code is input on DQ0. The operation is terminated by the PROGRAM/ERASE RESUME command. PROGRAM/ERASE SUSPEND command enables the memory controller to interrupt and suspend an array PROGRAM or ERASE operation within the program/erase latency.

If a SUSPEND command is issued during a PROGRAM operation, then the flag status register bit 2 is set to 1. After erase/program latency time, the flag status register bit 7 is also set to 1, showing the device to be in a suspended state, waiting for any operation If a SUSPEND command is issued during an ERASE operation, then the flag status register bit 6 is set to 1. After erase/program latency time, the flag status register bit 7 is also set to 1, showing that device to be in a suspended state, waiting for any operation.

If the time remaining to complete the operation is less than the suspend latency, the device completes the operation and clears the flag status register bits 2 or 6, as applicable. Because the suspend state is volatile, if there is a power cycle, the suspend state information is lost and the flag status register powers up as 80h. During an ERASE SUSPEND operation, a PROGRAM or READ operation is possible in any sector except the one in a suspended state. Reading from a sector that is in a suspended state will output indeterminate data. The device ignores a PROGRAM command to a sector that is in an ERASE SUSPEND state; it also sets the flag status register bit 4 to 1: program failure/protection error, and leaves the write enable latch bit unchanged.

8.18 Program/Erase Resume (PER) (7Ah)

To initiate the PROGRAM/ERASE RESUME command, S# is driven LOW. The command code is input on DQ0. The operation is terminated by driving S# HIGH. When this command is executed, the status register write in progress bit is set to 1, and the flag status register program erase controller bit is set to 0. This command is ignored if the device is not in a suspended state.

8.19 Program OTP Array Command (42h)

To initiate the PROGRAM OTP ARRAY command, the WRITE ENABLE command must be issued to set the write enable latch bit to 1; otherwise, the PROGRAM OTP ARRAY command is ignored and flag status register bits are not set. S# is driven LOW and held LOW until the eighth bit of the last data byte has been latched in, after which it must be driven HIGH. The command code is input on DQ0, followed by three bytes and at least one data byte. Each address bit is latched in during the rising edge of the clock. When S# is driven HIGH, the operation, which is self-timed, is initiated; its duration is tPOTP. There is no rollover mechanism; therefore, after a maximum of 65 bytes are latched in and subsequent bytes are discarded.

PROGRAM OTP ARRAY programs, at most, 64 bytes to the OTP memory area and one OTP control byte. When the operation is in progress, the write in progress bit is set to 1. The write enable latch bit is cleared to 0, whether the operation is successful or not, and the status register and flag status register can be polled for the operation status. When the operation completes, the write in progress bit is cleared to 0.

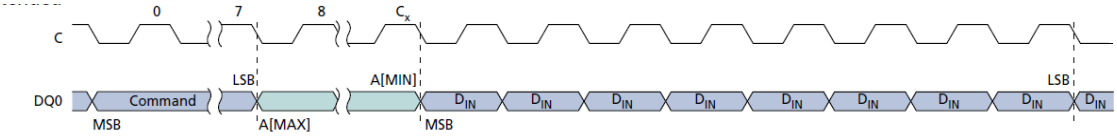


Figure 23. Program OTP Array command Sequence Diagram

8.20 Read OTP Command (48h)

To initiate a READ OTP ARRAY command, S# is driven LOW. The command code is input on DQ0, followed by three bytes and dummy clock cycles. Each address bit is latched in during the rising edge of C. Data is shifted out on DQ1, beginning from the specified address and at a maximum frequency of fC (MAX) on the falling edge of the clock.

The address increments automatically to the next address after each byte of data is shifted out. There is no rollover mechanism; therefore, if read continuously, after location 40h, the device continues to output data at location 40h. The operation is terminated by driving S# HIGH at any time during data output.

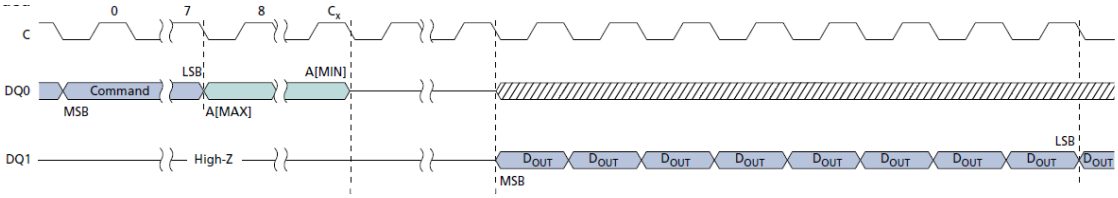


Figure 24. Read OTP command Sequence Diagram

OTP Control Byte (Byte 64)

Bit	Name	Settings	Description
0	OTP control byte	0 = Locked 1 = Unlocked (Default)	Used to permanently lock the OTP array (byte 64). When bit 0 = 1, the OTP array can be programmed. When bit 0 = 0, the OTP array is read only. Once bit 0 has been programmed to 0, it can no longer be changed to 1. PROGRAM OTP ARRAY is ignored, write enable latch bit remains set, and flag status register bits 1 and 4 are set.

8.21 CLEAR FLAG STATUS REGISTER Command

To execute the CLEAR FLAG STATUS REGISTER command and reset the error bits (erase, program, and protection), S# is driven LOW. For extended SPI protocol, the command code is input on DQ0. For dual SPI protocol, the command code is input on DQ[1:0]. For quad SPI protocol, the command code is input on DQ[3:0]. The operation is terminated by driving S# HIGH at any time.

9 ELECTRICAL CHARACTERISTICS

9.1 Power-up Timing

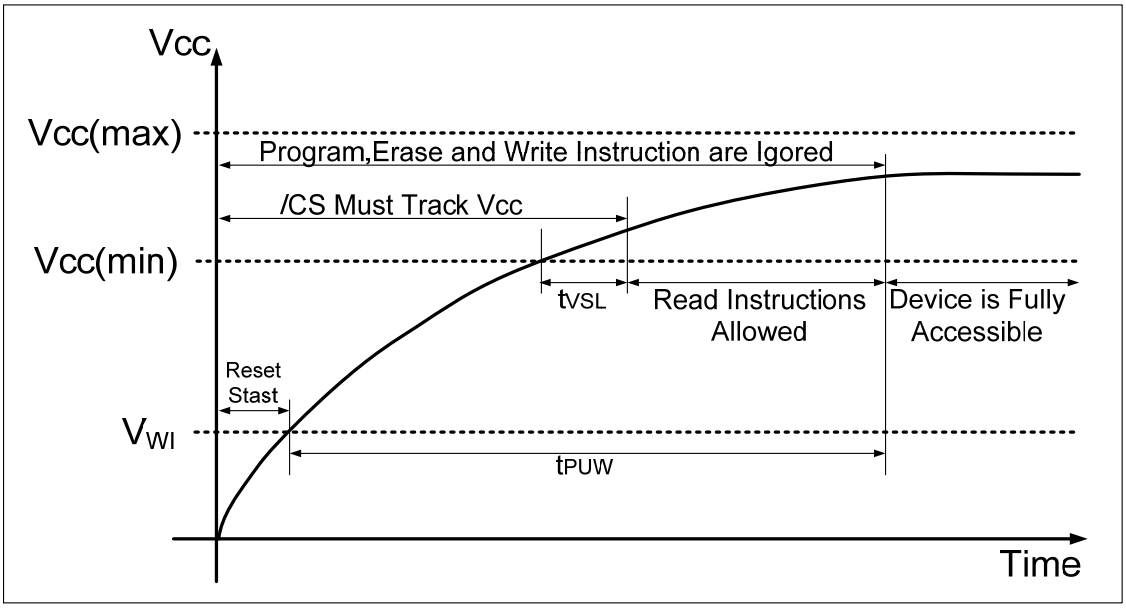


Figure 25, Power-up Timing

Table 6, Power-up Timing

PARAMETER	SYMBOL	TYPE		UNIT
		MIN	MAX	
Vcc(min) to CS# Low	tVSL(1)	10		μs
Time Delay Before Write Instruction	tPUW(1)	1	10	ms
Write Inhibit Threshold Voltage	VWI(1)	1	2	V

Note:
1.The parameters are characterized only.
2. VCC (max.) is 3.6V and VCC (min.) is 2.7V

9.2 Absolute Maximum Ratings

Stresses above the values so mentioned above may cause permanent damage to the device. These values are for a stress rating only and do not imply that the device should be operated at conditions up to or above these values.

Table 7, Absolute Maximum Ratings

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		-0.6 to +4.0	V
Voltage applied on any pin	V_{IO}	Relative to Ground	-0.6 to VCC+0.4	V
Transient Voltage on any Pin	V_{IOT}	<20ns Transient Relative to Ground	-2.0 to VCC+2.0	V
Storage Temperature	T_{STG}		-65 to +150	℃
Lead Temprature	T_{LEAD}		See Note(3)	℃
Electrostatic Discharge Voltage	V_{ESD}	Human Body Model(4)	-2000 to +2000	V

Notes:
1. Specification for ZD25Q64 is preliminary. See preliminary designation at the end of this document.
2. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
3. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
4. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 ohms, R2=500 ohms).

9.3 INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1(each byte contains FFH). The Status Register bits are set to 0.

9.4 Recommended Operating Ranges

Table 8, Recommended Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage	VCC	FR=104MHz,fR=50MHz	2.7	3.6	V
Ambient Temperature, Operating	TA	Industrial	-40	+85	℃

Notes: 1. Recommended Operating Ranges define those limits between which the functionality of the device is guaranteed.

9.5 DC Characteristics

Table 9. DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
CIN(1)	Input Capacitance	VIN = 0V(2)			6	pF
Cout(1)	Output Capacitance	VOUT = 0V(2)			8	pF
ILI	Input Leakage				±2	µA
ILO	I/O Leakage				±2	µA
ICC1	Standby Current	CS# = VCC, VIN = GND or VCC			100	µA
ICC3	Current Read Data / Dual Output Read 33MHz(2)	C = 0.1 VCC / 0.9 VCC DO = Open			6	mA
ICC3	Current Read Data / Dual Output Read 108MHz(2)	C = 0.1 VCC / 0.9 VCC DO = Open			18	mA
ICC4	Current Page Program	CS# = VCC			20	mA
ICC5	Current Write Status Register	CS# = VCC			20	mA
ICC6	Current Sector/Block Erase	CS# = VCC			20	mA
ICC7	Current Chip Erase	CS# = VCC			20	mA
VIL	Input Low Voltage		–0.5		VCC x 0.2	V
VIH	Input High Voltage		VCC x0.7		VCC +0.4	V
VOL	Output Low Voltage	IOL = 1.6 mA	VSS		0.4	V
VOH	Output High Voltage	IOH = –100 µA	VCC –0.2		VCC	V

Notes:
1. Tested on sample basis and specified through design and characterization data. TA=25° C, VCC 3V.
2. Checker Board Pattern.

9.6 AC Measurement Conditions

Table 10, AC Measurement Conditions

Symbol	PARAMETER	Min.	Max.	Unit
CL	Load Capacitance		30	pF
TR, TF	Input Rise and Fall Times		5	ns
VIN	Input Pulse Voltages	0.2VCC to 0.8VCC		V
VtIN	Input Timing Reference Voltages	0.3VCC to 0.7VCC		V
VtON	Output Timing Reference Voltages	0.5 VCC to 0.5 VCC		V

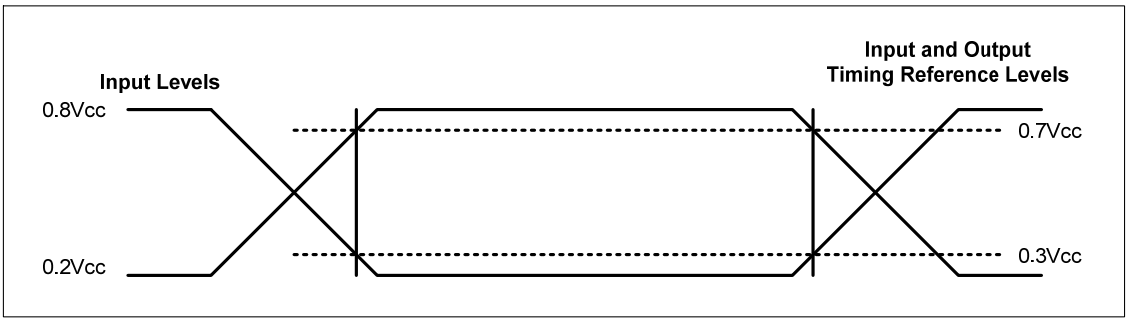


Figure 44, AC Measurement I/O Waveform

9.7 AC Electrical Characteristics

Table 11, AC Electrical Characteristics

SYMBOL	ALT	Parameter	SPEC			UNIT
			MIN	TYP	MAX	
FR	fC	Clock frequency For all instructions, except Read Data (03h) and Dual output(3bh) 2.7V-3.6V VCC & Industrial Temperature	D.C.		108	MHz
fR		Clock freq. Read Data instruction (03h)	D.C.		50	MHz
tCLH, tCLL(1)		Clock High, Low Time for all instructions except Read Data (03h)	4			Ns
tCRLH, tCRLL(1)		Clock High, Low Time for Read Data (03h) instruction	4			Ns
tCLCH(2)		Clock Rise Time peak to peak	0.1			V/ns
tCHCL(2)		Clock Fall Time peak to peak	0.1			V/ns
tSLCH	tCSS	CS# Active Setup Time relative to CLK	4			Ns
tCHSL		CS# Not Active Hold Time relative to CLK	4			Ns
tDVCH	tDSU	Data In Setup Time	2			Ns
tCHDX	tDH	Data In Hold Time	3			Ns
tCHSH		CS# Active Hold Time relative to CLK	4			Ns
tSHCH		CS# Not Active Setup Time relative to CLK	4			Ns
tSHSL	tCSH	CS# Deselect Time (for Array Read →Array Read / Erase or Program → Read Status Register)	20/50			Ns
tSHQZ(2)	tDIS	Output Disable Time			8	Ns
tCLQV	tV	Clock Low to Output Valid 2.7V-3.6V / 3.0V-3.6V			7	Ns
tCLQX	tHO	Output Hold Time	1			Ns
tHLCH		/HOLD Active Setup Time relative to CLK	4			Ns
tCHHH		/HOLD Active Hold Time relative to CLK	4			Ns
tHHCH		/HOLD Not Active Setup Time relative to CLK	4			Ns
tCHHL		/HOLD Not Active Hold Time relative to CLK	4			Ns
tHHQX(2)	tLZ	/HOLD to Output Low-Z			8	Ns
tHLQZ(2)	tHZ	/HOLD to Output High-Z			8	Ns
tWHSL(3)		Write Protect Setup Time Before CS# Low	20			Ns
tSHWL(3)		Write Protect Hold Time After CS# High	100			Ns
tW		Write Status Register Time		1.3	8	Ms
tWNVCR		Write NONVOLATILE CONFIGURATION REGISTER cycle time		0.2	3	s
tCFSR		CLEAR FLAG STATUS REGISTER cycle time		40		Ns
tWVCR		WRITE VOLATILE CONFIGURATION REGISTER cycle time		40		Ns
tPP		Page Program Time		0.5	5	Ms
tSE		Sector Erase Time (4KB)		0.25	0.8	S
tBE		Block Erase Time (64KB)		0.6	3	S
tCE		Chip Erase Time		60	120	S

Notes:
1, Clock high + Clock low must be less than or equal to 1/fC.
2, Value guaranteed by design and/or characterization, not 100% tested in production.
3, Only applicable as a constraint for a Write Status Register instruction when Sector Protect Bit is set to 1.
4, For multiple bytes after first byte within a page, tBPN = tBP1 + tBP2 * N (typical) and tBPN = tBP1 + tBP2 * N (max), where N = number of bytes programmed.

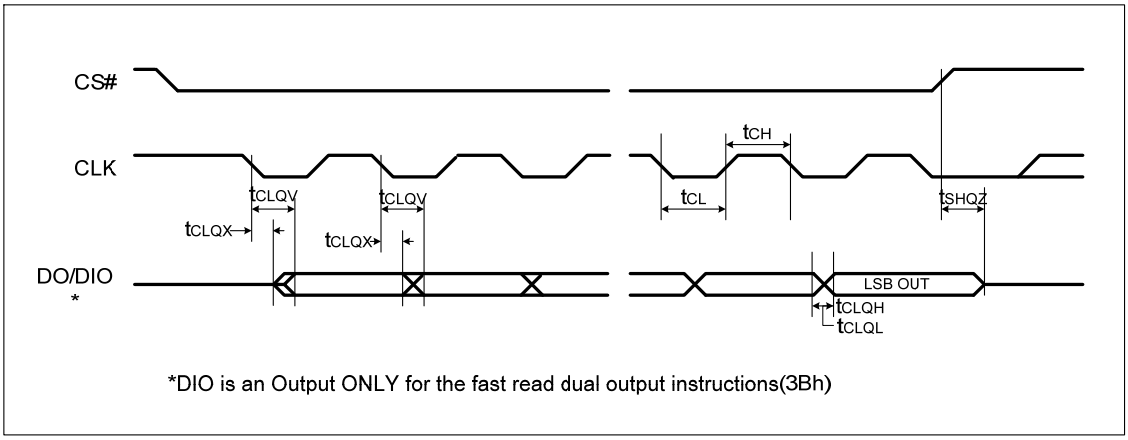


Figure 45, Serial Output Timing

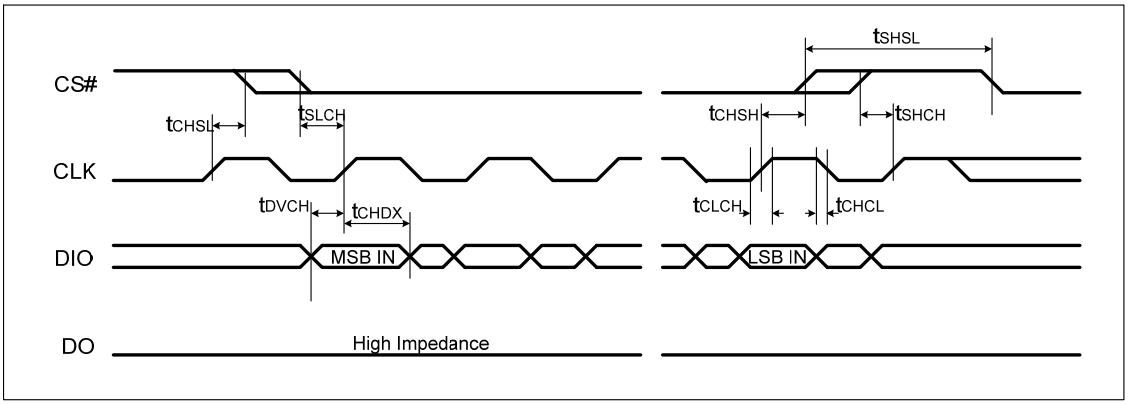


Figure 46, Input Timing

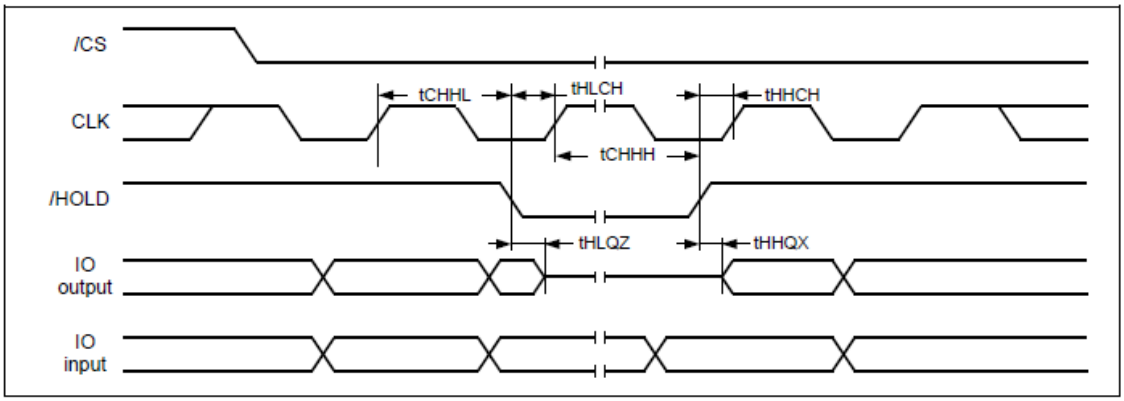
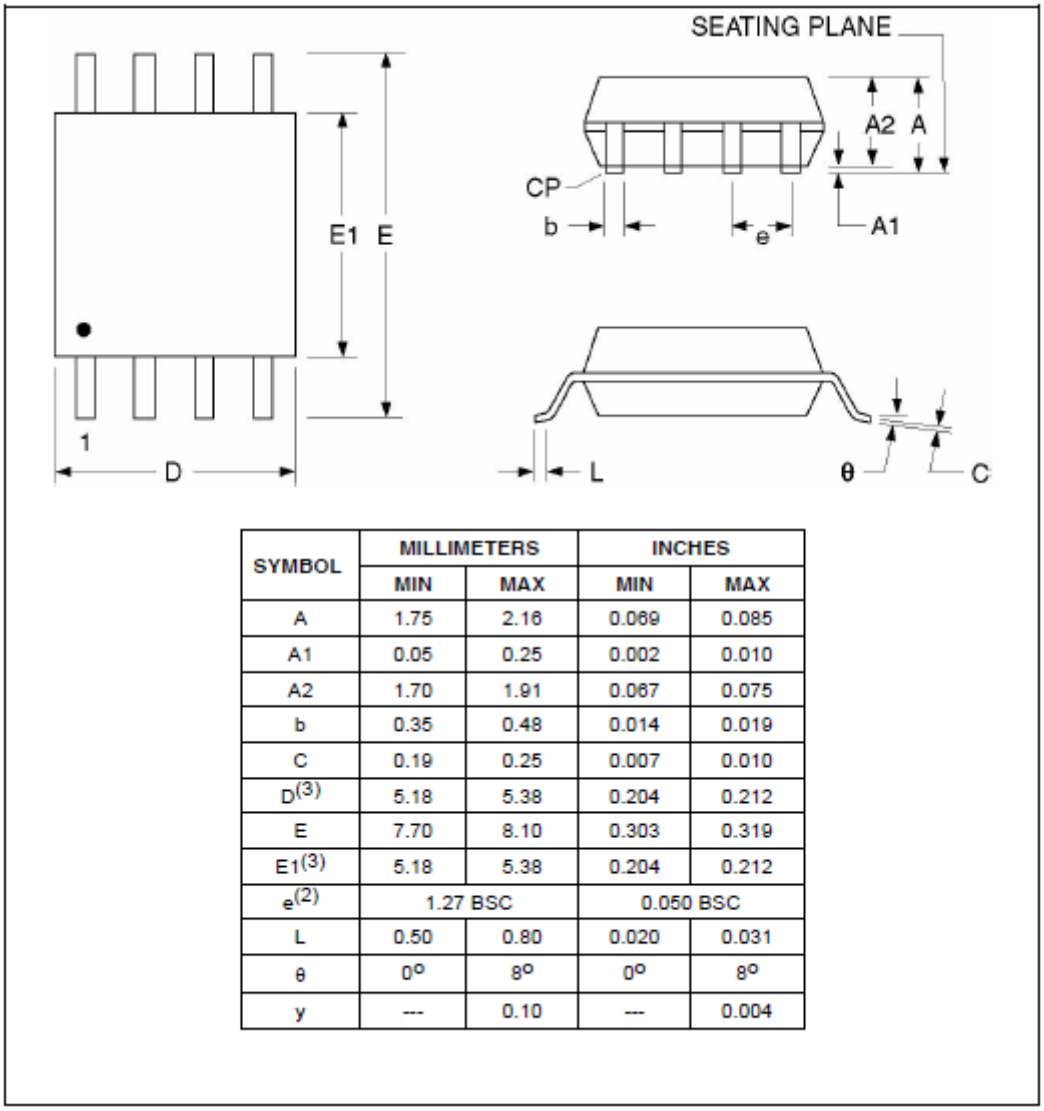


Figure 47, Hold Timing

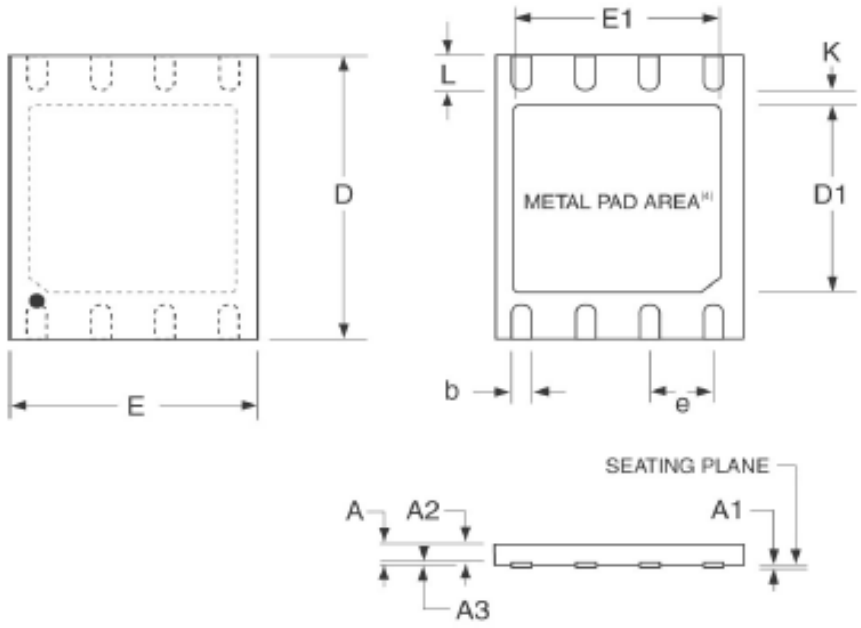
10 PACKAGE MECHANICAL

10.1 8-Pin SOIC 208-mil



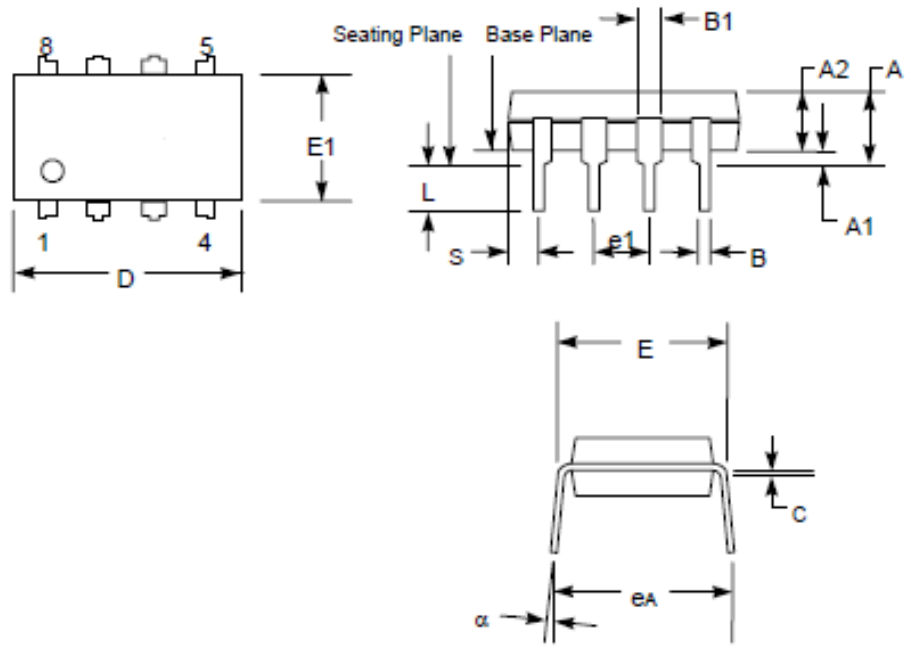
SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.75	2.16	0.069	0.085
A1	0.05	0.25	0.002	0.010
A2	1.70	1.91	0.067	0.075
b	0.35	0.48	0.014	0.019
C	0.19	0.25	0.007	0.010
D(3)	5.18	5.38	0.204	0.212
E	7.70	8.10	0.303	0.319
E1(3)	5.18	5.38	0.204	0.212
e(2)	1.27 BSC		0.050 BSC	
L	0.50	0.80	0.020	0.031
θ	0°	8°	0°	8°
y	---	0.10	---	0.004

10.2 8-Contact WSON (6x5mm)



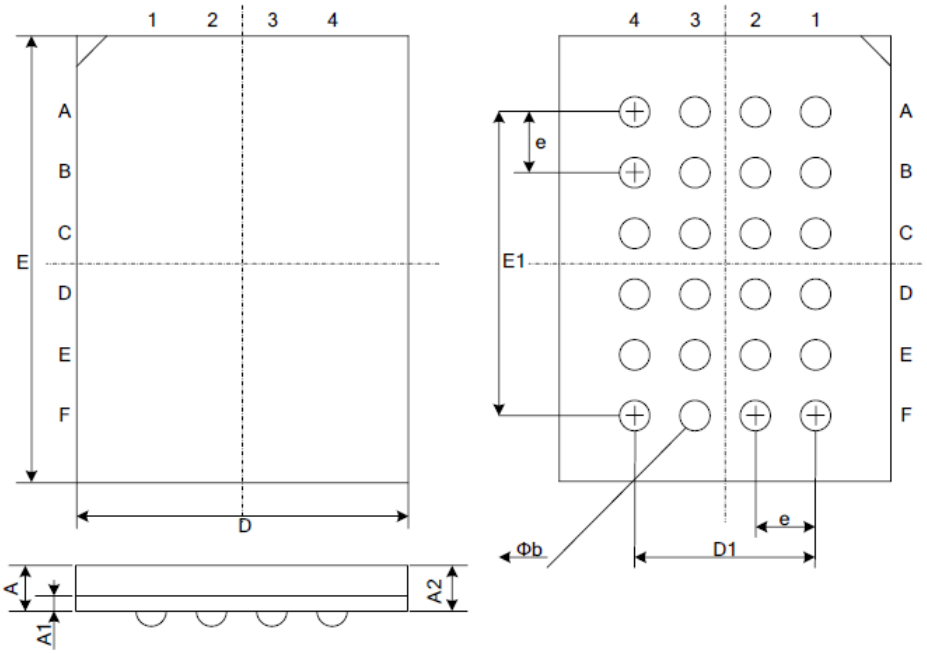
SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP.	MAX	MIN	TYP.	MAX
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	0.02	0.05	0.0000	0.0008	0.0019
A2		0.55			0.0126	
A3	0.19	.0.20	0.25	0.0075	0.0080	0.0098
b	0.36	0.40	0.48	0.0138	0.0157	0.0190
D(3)	5.90	6.00	6.10	0.2320	0.2360	0.2400
D1	3.30	3.40	3.50	0.1299	0.1338	0.1377
E	4.90	5.00	5.10	0.1930	0.1970	0.2010
E1(3)	4.20	4.30	4.40	0.1653	0.1692	0.1732
e(2)	1.27 BSC			0.0500 BSC		
K	0.20			0.0080		
L	0.50	0.60	0.75	0.0197	0.0236	0.0295

10.3 8-Pin PDIP 300-mil



SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP.	MAX	MIN	TYP.	MAX
A	---	---	5.33	---	---	0.210
A1	0.38	---	---	0.015	---	---
A2	3.18	3.30	3.43	0.125	0.130	0.135
B	0.41	0.46	0.56	0.016	0.018	0.022
B1	1.47	1.52	1.63	0.058	0.060	0.064
c	0.20	0.25	0.36	0.008	0.010	0.014
D	9.02	9.27	10.16	0.355	0.365	0.400
E	7.37	7.62	7.87	0.290	0.300	0.310
E1	6.22	6.35	6.48	0.245	0.250	0.255
e1	2.29	2.54	2.79	0.090	0.100	0.110
L	2.92	3.30	3.81	0.115	0.130	0.150
α	0	7	15	0	7	15
e_A	8.51	9.02	9.53	0.335	0.355	0.375
S	---	---	1.14	---	---	0.045

10.4 TFBGA-24BALL (6*4 ball array)

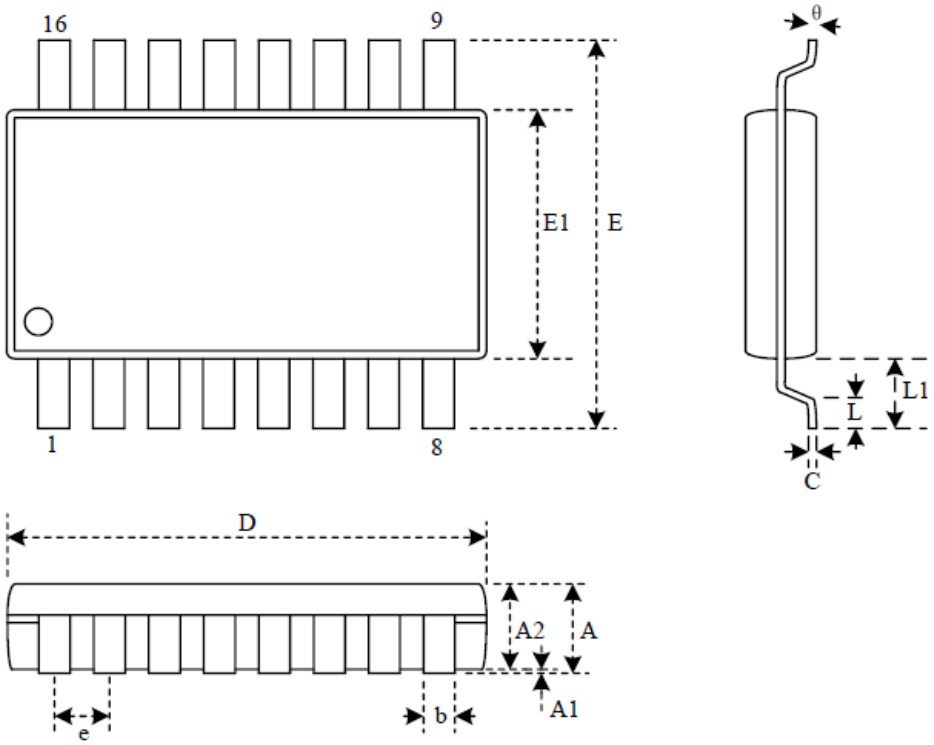


Dimensions

Symbol / Unit		A	A1	A2	b	D	D1	E	E1	e
mm	Min		0.25		0.35	5.90		7.90		
	Nom		0.30	0.85	0.40	6.00	3.00	8.00	5.00	1.00
	Max	1.20	0.35		0.45	6.10		8.10		
Inch	Min		0.010		0.014	0.232		0.311		
	Nom		0.012	0.033	0.016	0.236	0.120	0.315	0.200	0.039
	Max	0.047	0.014		0.018	0.240		0.319		

Note: Both package length and width do not include mold flash.

10.5 SOP16 300mil



Dimensions

Symbol / Unit		A	A1	A2	b	C	D	E	E1	e	L	L1	θ
mm	Min	2.36	0.10	2.24	0.36	0.20	10.10	10.10	7.42		0.40	1.31	0
	Nom	2.55	0.20	2.34	0.41	0.25	10.30	10.35	7.52	1.27BSC	0.84	1.44	5
	Max	2.75	0.30	2.44	0.51	0.30	10.50	10.60	7.60		1.27	1.57	8
Inch	Min	0.093	0.004	0.088	0.014	0.008	0.397	0.397	0.292		0.016	0.052	0
	Nom	0.100	0.008	0.092	0.016	0.010	0.405	0.407	0.296	0.050BSC	0.033	0.057	5
	Max	0.108	0.012	0.096	0.020	0.012	0.413	0.417	0.299		0.050	0.062	8

Note:Both package length and width do not include mold flash.

11 REVISION LIST

Version No.	Description	Date
A	Initial Release	2016/04/19